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| 12 | DDR II DIMM 3 & 4 |
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| 14 | nVidia MCP55 - HT / PCI / LPC |
| 15 | nVidia MCP55 - PCI-E |
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| 18 | nVidia MCP55 - PWR & GND |
| 19 | NB PCI-E x16 Pri / Sec Slot |
| 20 | SB PCI-E x16 Pri / Sec Slot |
| 21 | SB PCI-E x1 / PCI Slot |
| 22 | Gigabit PHY - RTL8211B |
| 23 | 1394 Controller - JMB381 |
| 24 | |
| 25 | JMicron JMB363 |
| 26 | Super I/O - F71882FG |
| 27 | Fan Controller |
| 28 | uPI ACPI Solution |
| 29 | uPI Power Regulator |
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MS-7523

Version : 1.0 *Diamond Edition*

CPU :

Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 Sequence

System Chipset :

nVidia C73
nVidia MCP55P

On Board Chipset :

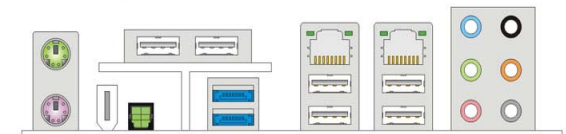
GB PHY 1 -- RealTek RTL8211BL
GB PHY 2 -- RealTek RTL8211BL
VRM 11 - Intersil ISL6322
ACPI Controller -- uPI Solution
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- FinTek F71882FG
SPI Flash 8Mb

Main Memory :

2 Channel DDR III* 4 (Max 8GB)

Expansion Slot :

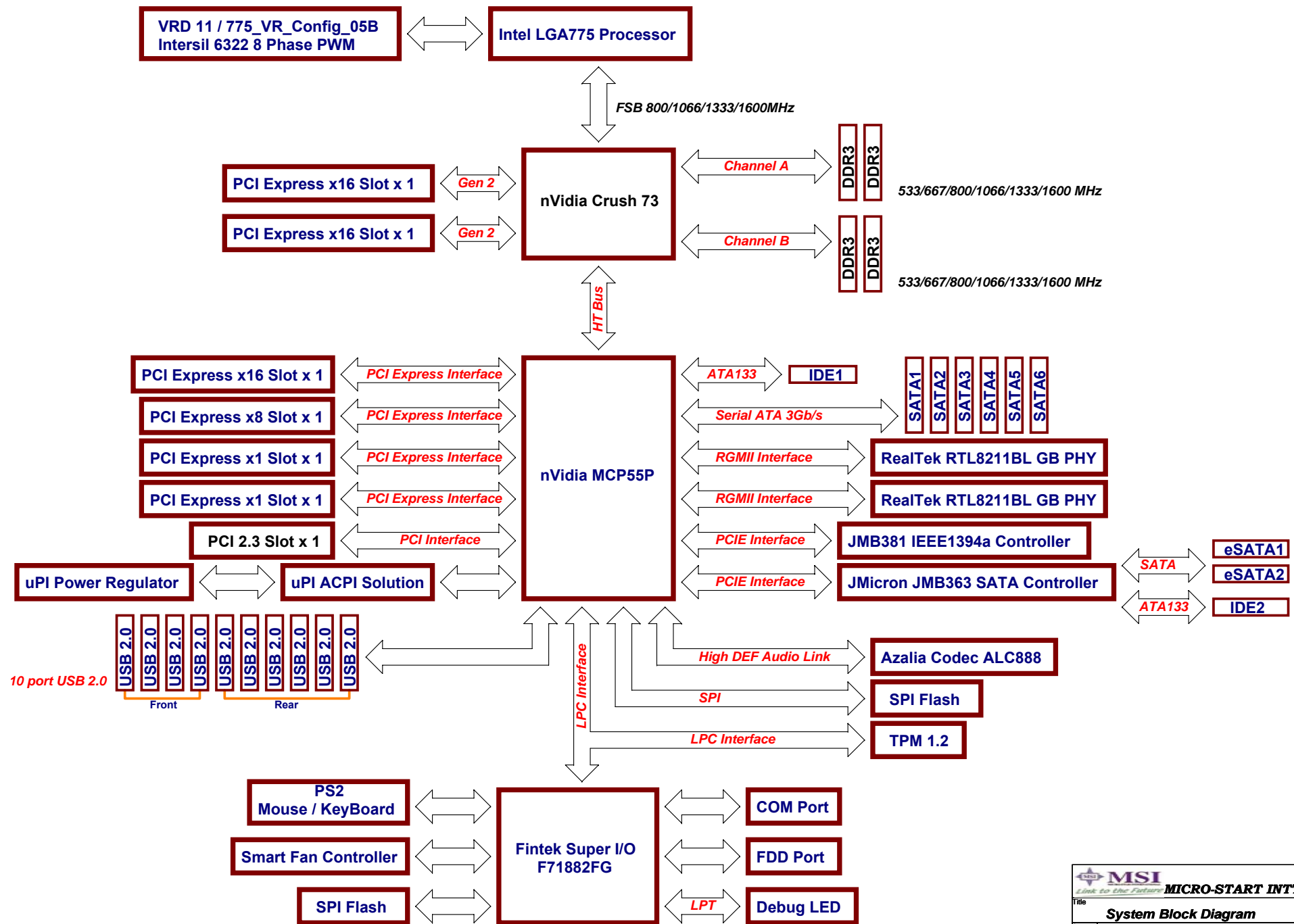
PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1



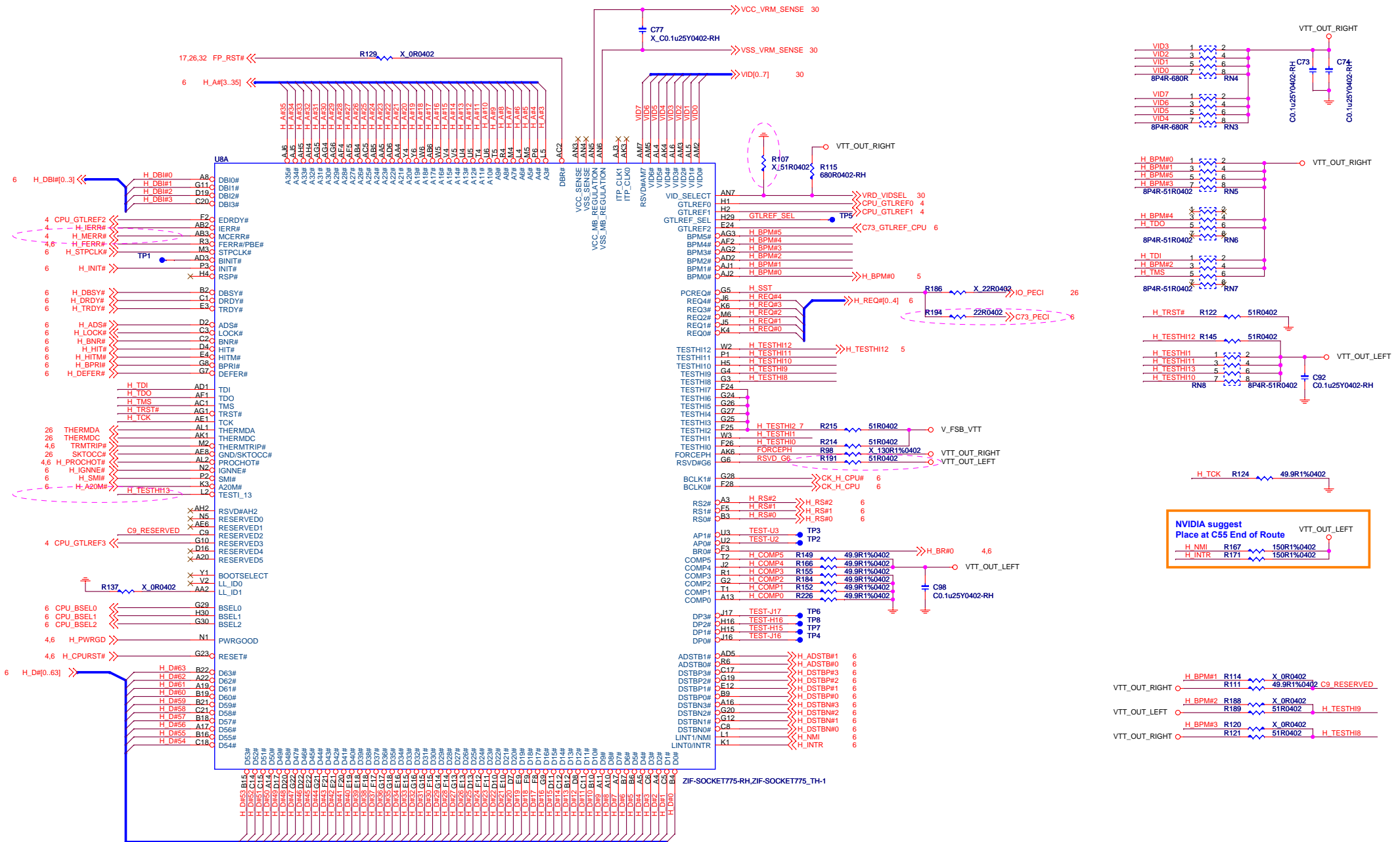
| ERP No. | Config Item | PlatForm or Option | Option Select |
|----------|-------------|---|---------------|
| 7510-01S | Cfg-STD | C55 + BR04 + MCP55P + ALC885 + RTL8211BP + JMB381 + JMB363 + F71882FG | STD |
| | | | |
| | | | |

| | | |
|---------------------------------|--------------------------------|----------------|
| MICRO-STAR INT'L CO.,LTD. | | |
| Title Cover Sheet | | |
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System Block Diagram



CPU LGA775 - Signals



CPU LGA775 - Power

CPU GTLREF Voltage Should be 0.63 x VTT = 0.756V

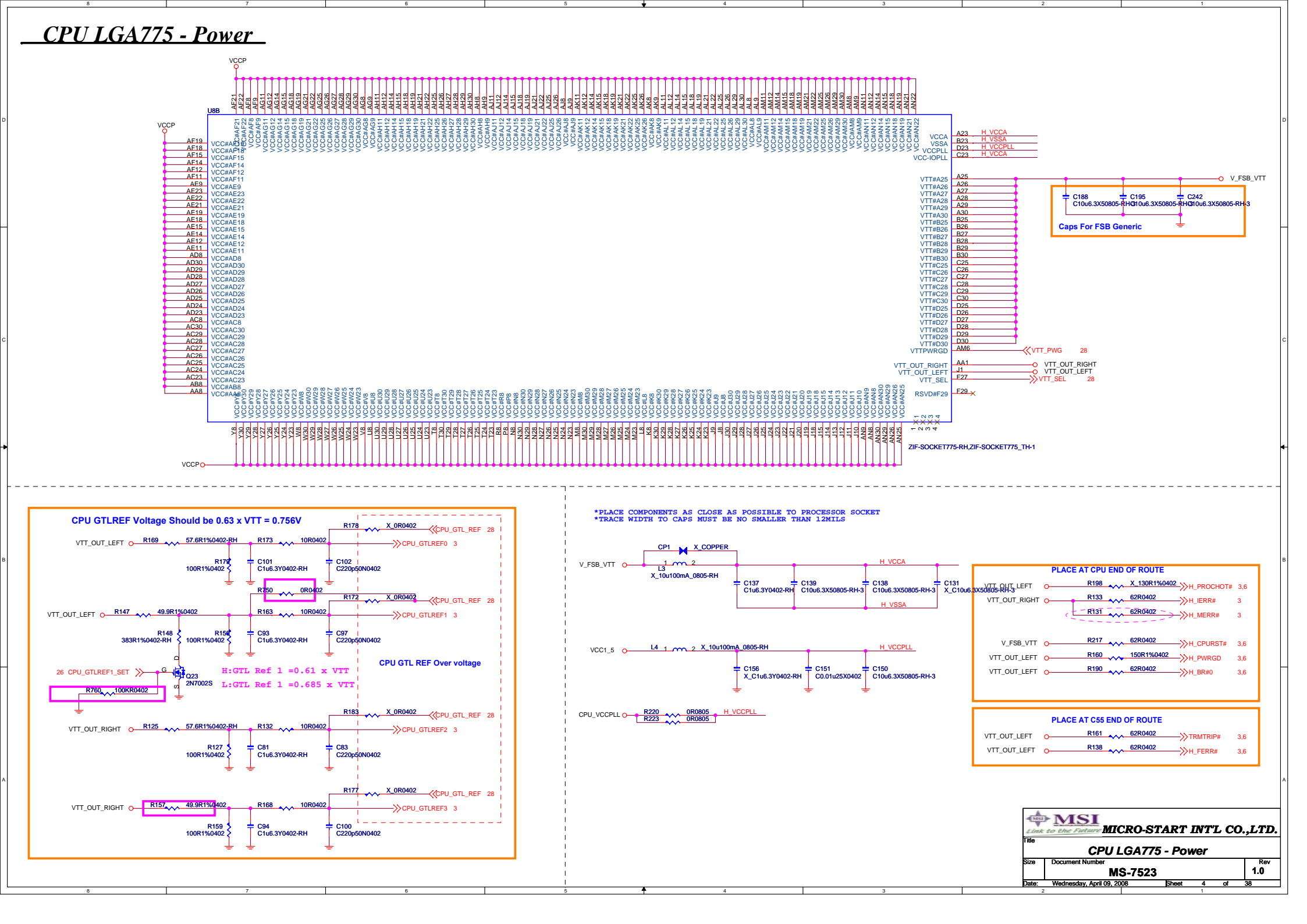
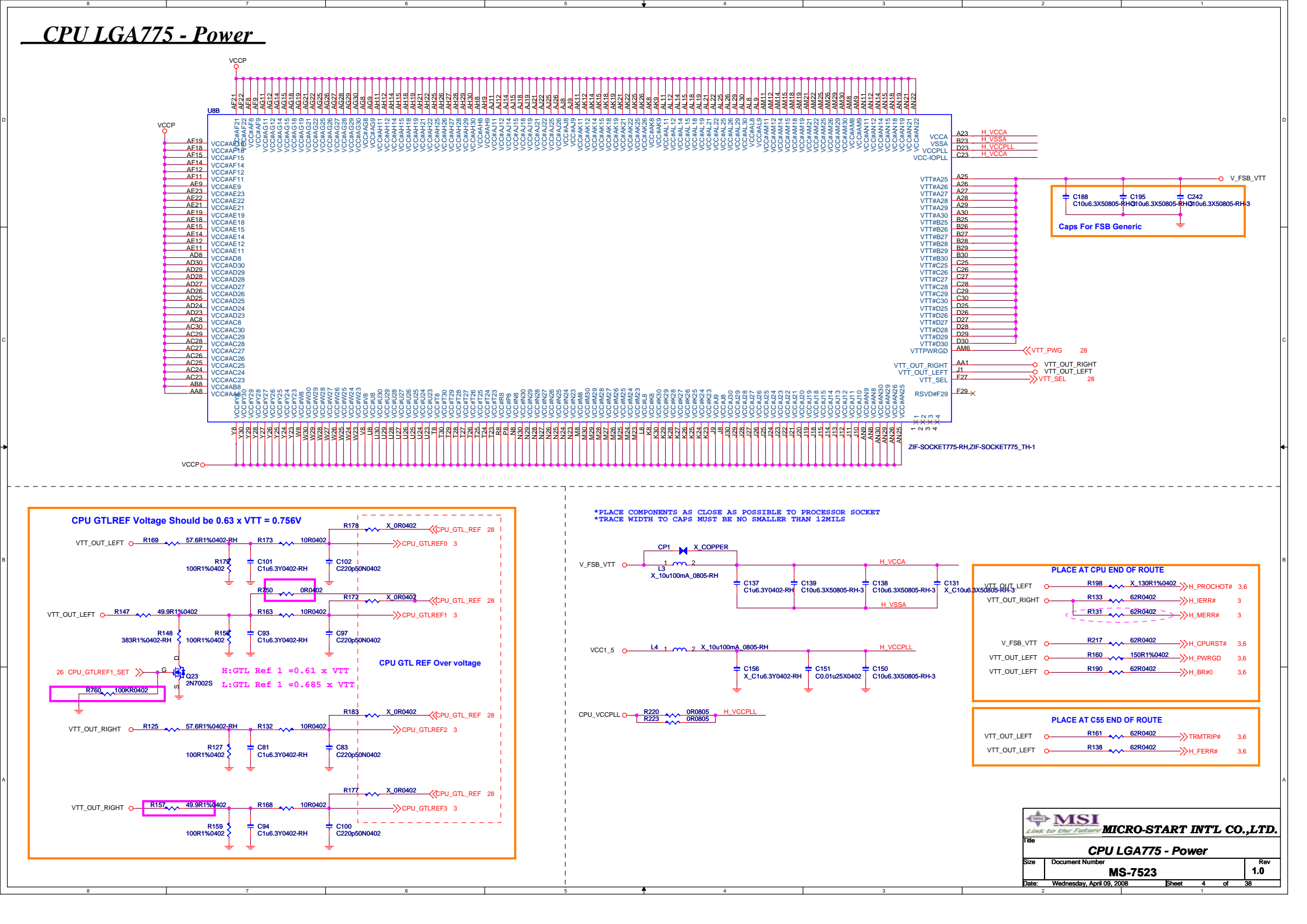
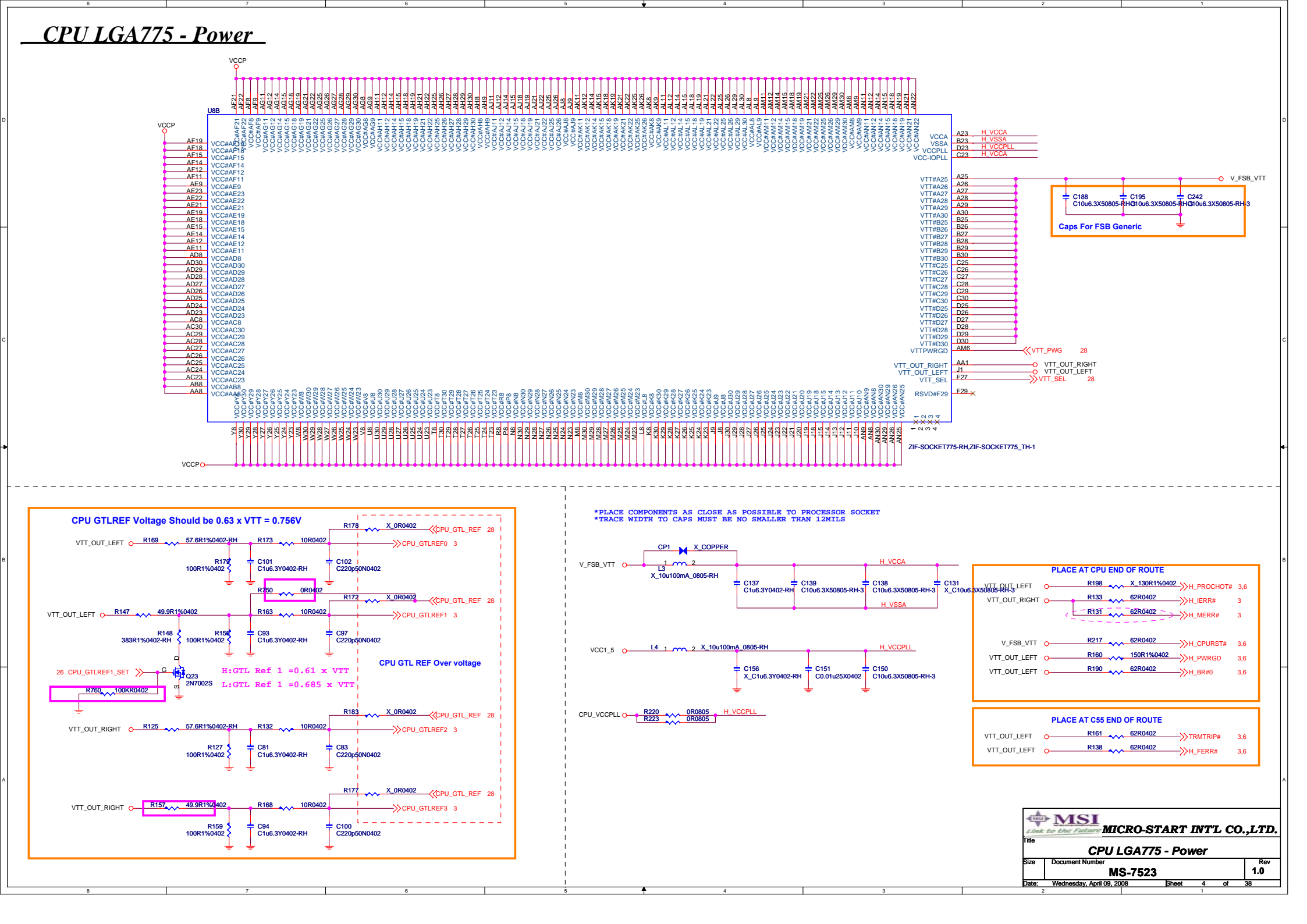
CPU GTL REF Over voltage

PLACE COMPONENTS AS CLOSE AS POSSIBLE TO PROCESSOR SOCKET
***TRACE WIDTH TO CAPS MUST BE NO SMALLER THAN 12MILLS**

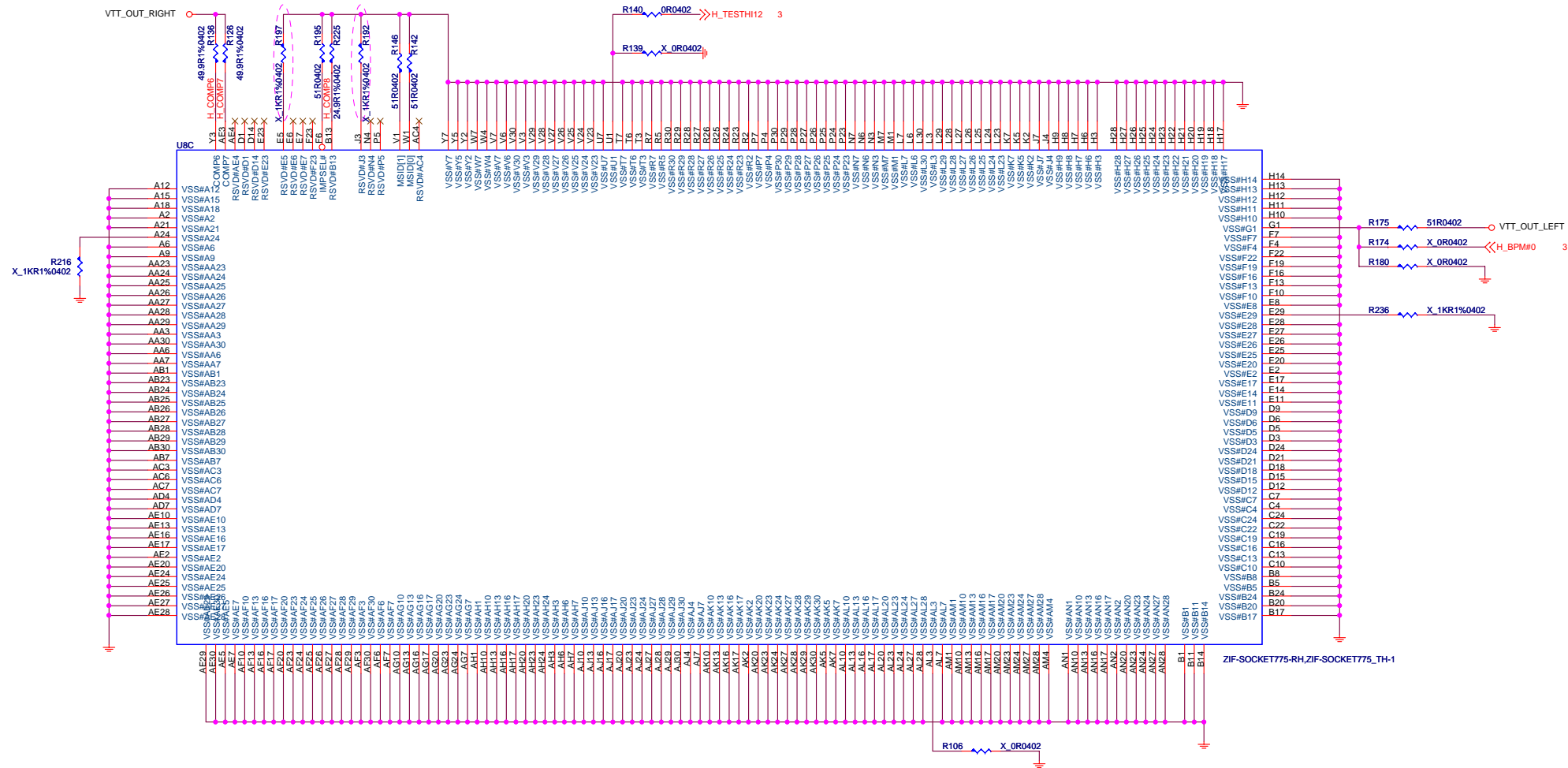
PLACE AT CPU END OF ROUTE

PLACE AT C55 END OF ROUTE

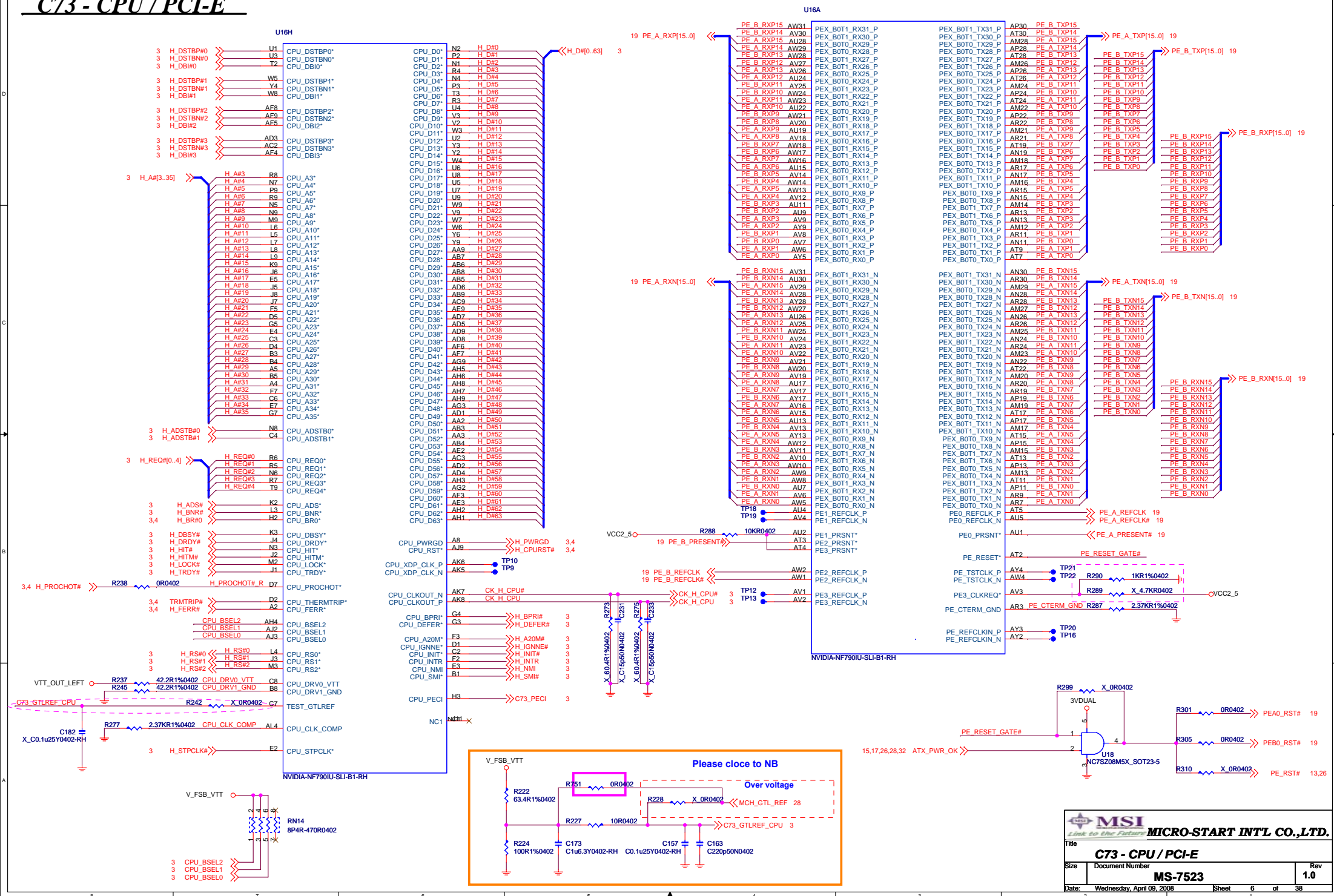
MSI MICRO-START INT'L CO.,LTD.
CPU LGA775 - Power
MS-7523
 Date: Wednesday, April 09, 2008 Sheet 4 of 38



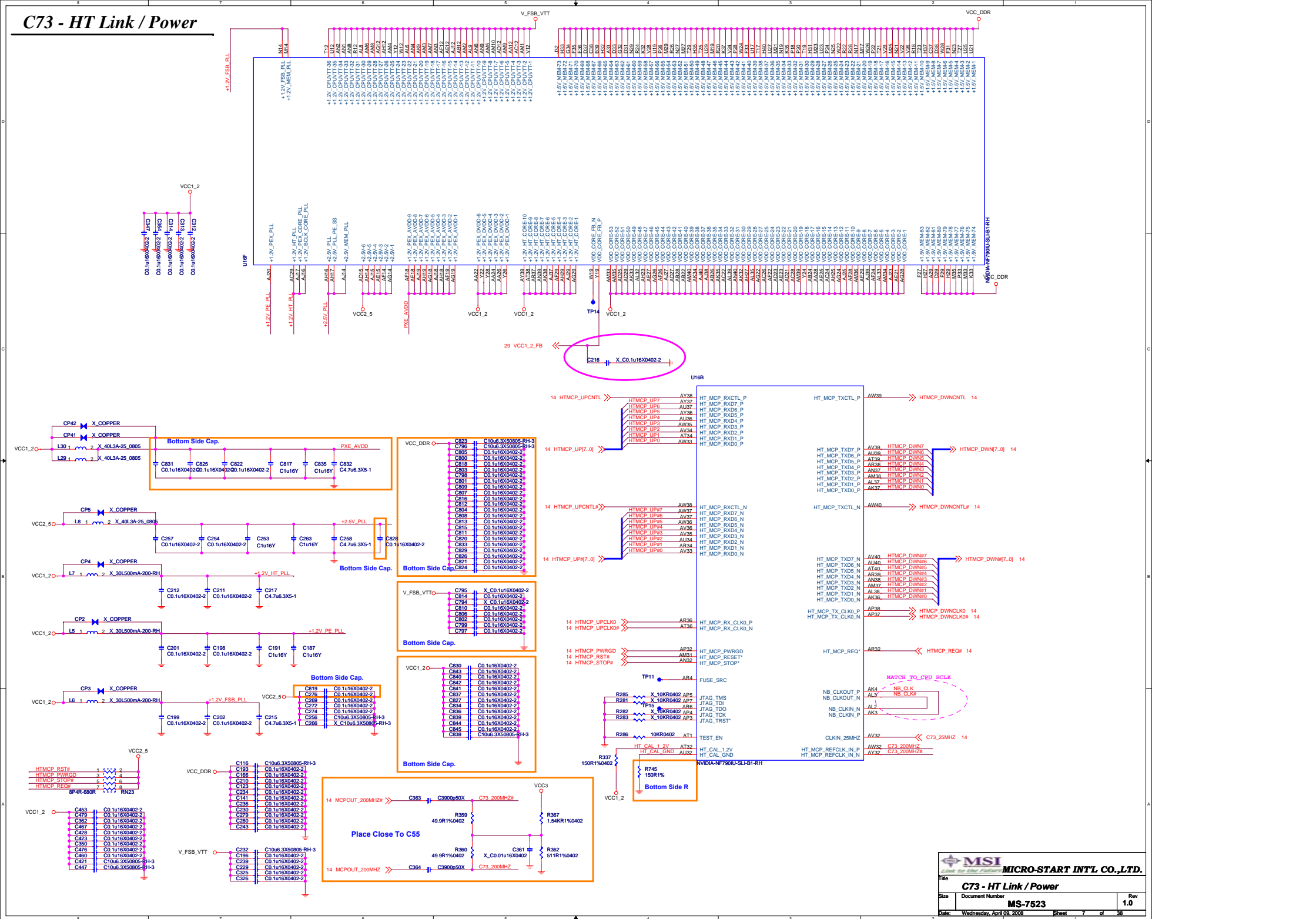
CPU LGA775 - Gnd



C73 - CPU / PCI-E

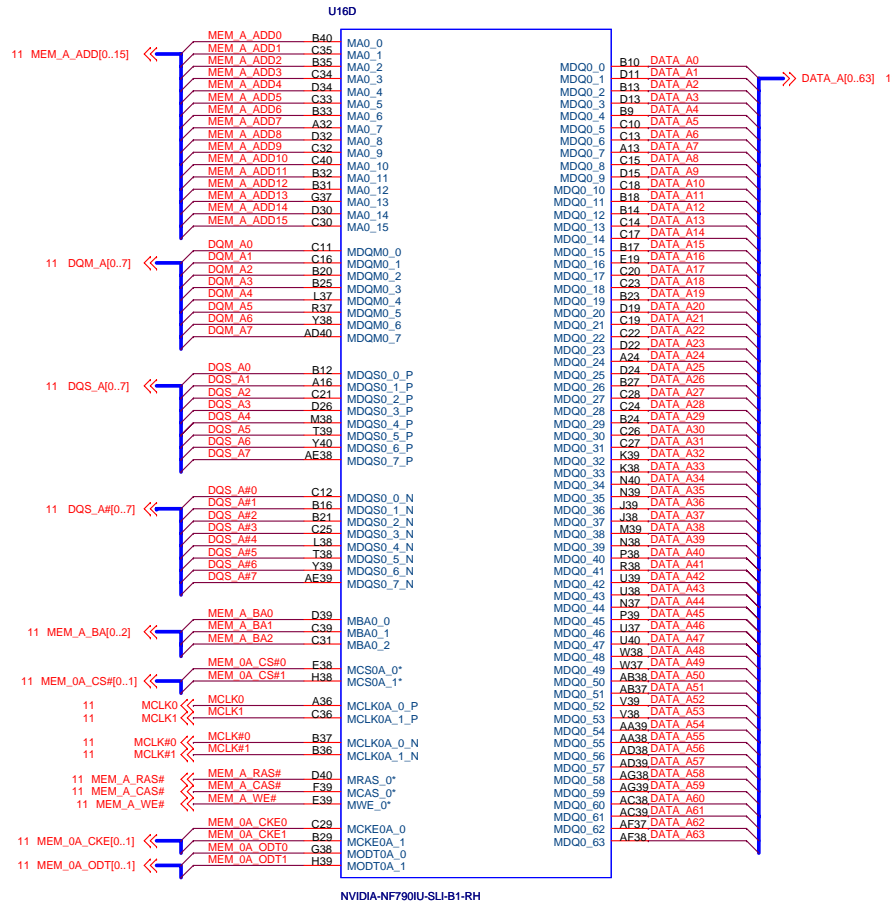


C73 - HT Link / Power

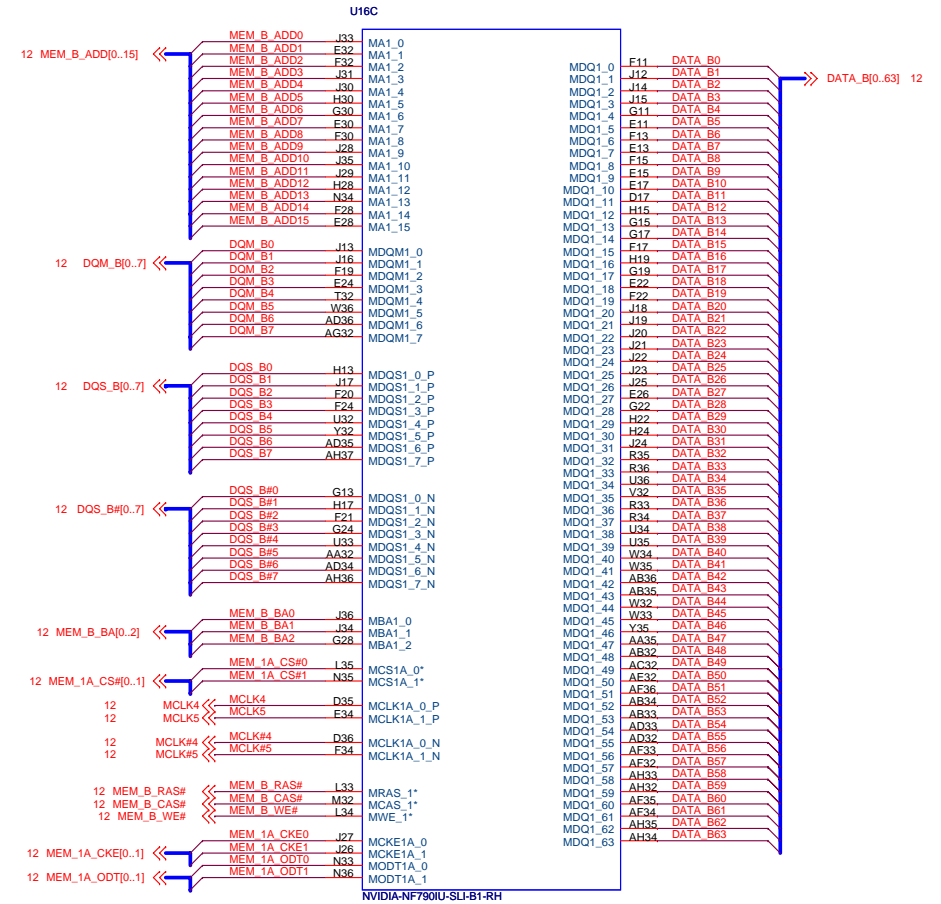


C73 - Memory A0

DIMM1 0A

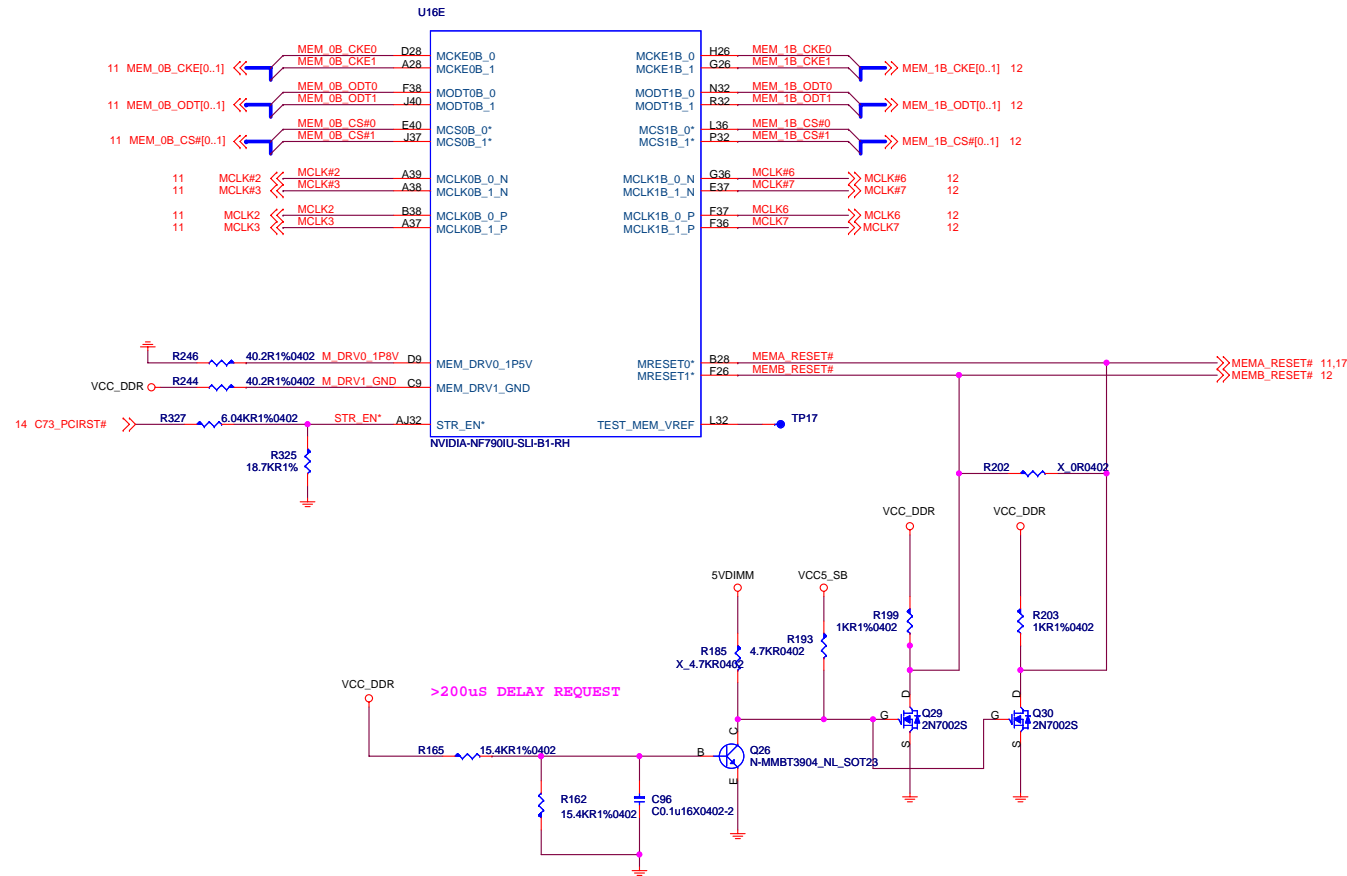


DIMM3 1A



C73 - Memory A1


DIMM2 0B / DIMM4 1B



| | | | |
|--------|--|--------|-------------------|
| DATA 0 | | DIMM 1 | ADDR 0A / CNTL 0A |
| | | DIMM 2 | ADDR 0B / CNTL 0B |
| DATA 1 | | DIMM 3 | ADDR 1A / CNTL 1A |
| | | DIMM 4 | ADDR 1B / CNTL 1B |

C73 - Gnd

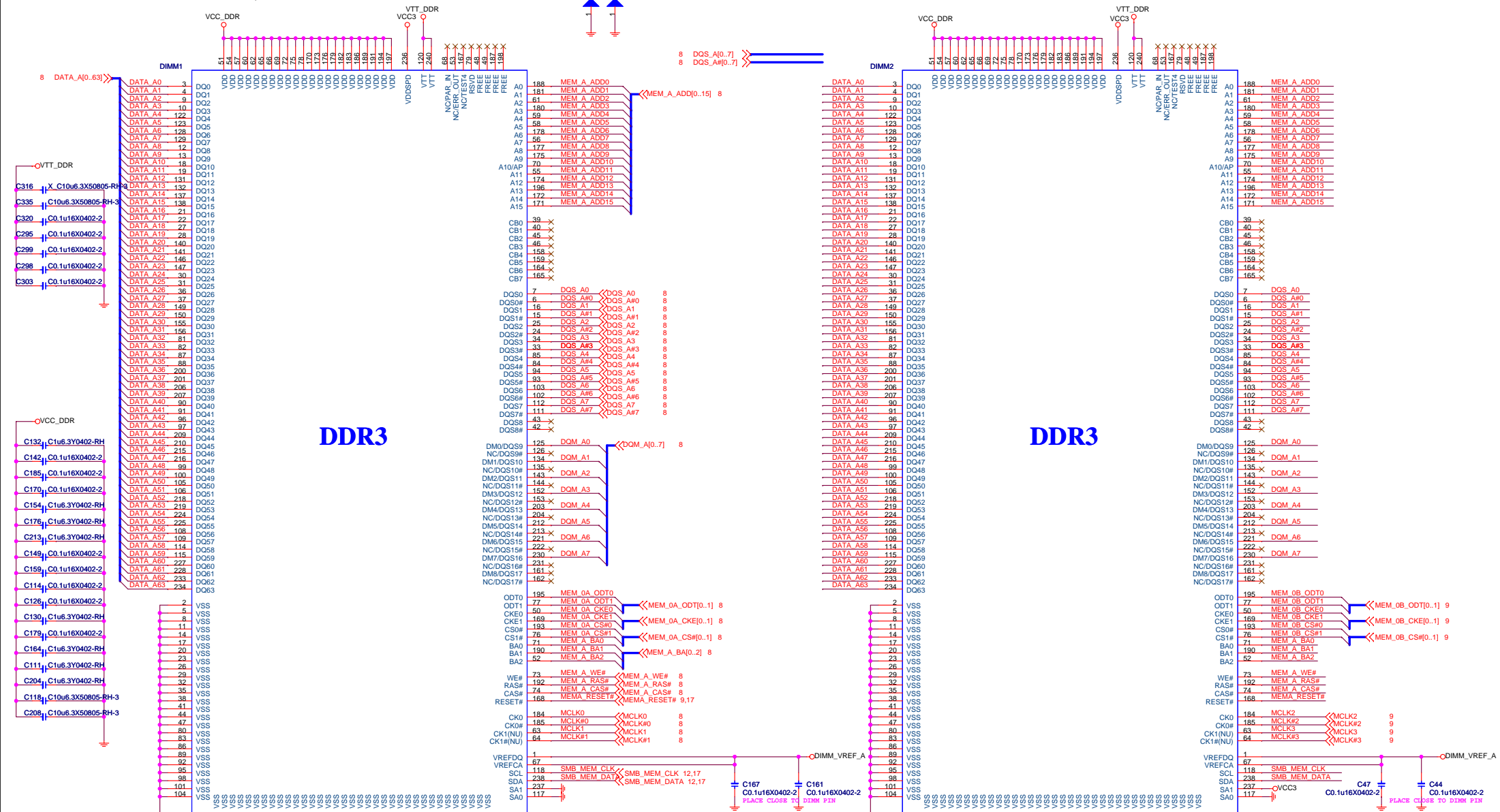


| | | |
|---|-----------------------------------|-------------------|
|  MICRO-START INT'L CO.,LTD. | | |
| Title C73 - Gnd | | |
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DDR3 DIMM1 / DIMM2

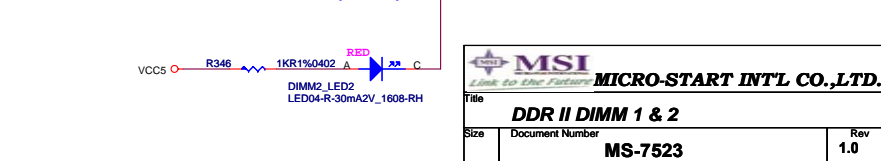
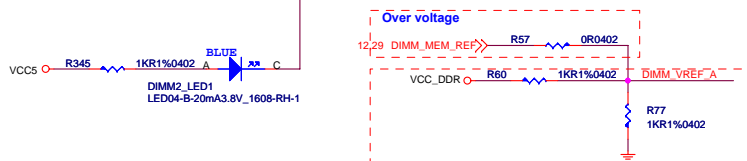
DDR3 DIMM1

DDR2 DIMM2

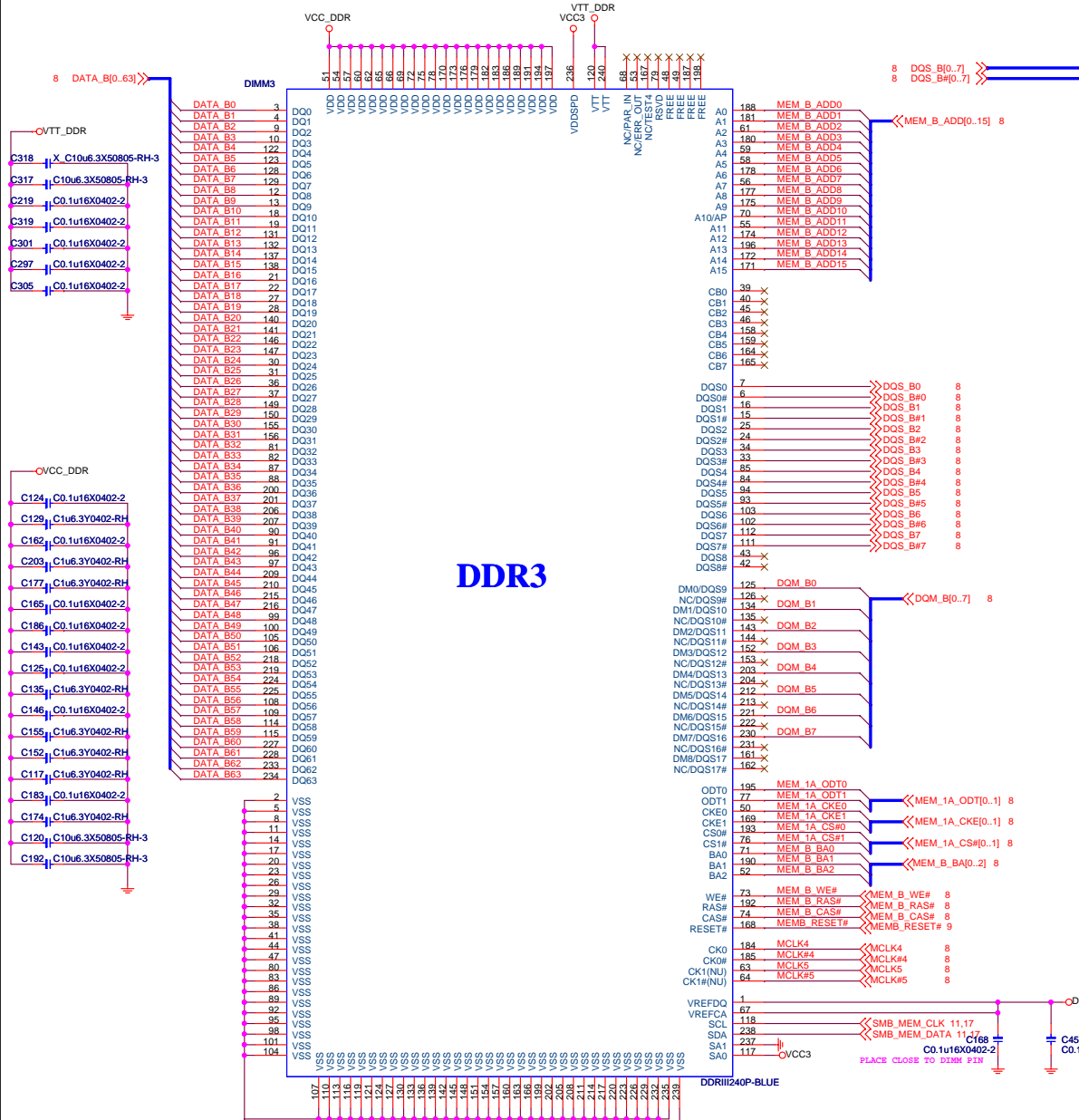


Address : 000 (0xA0)

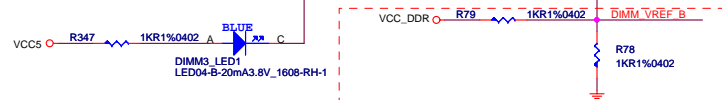
Address : 010 (0xA4)



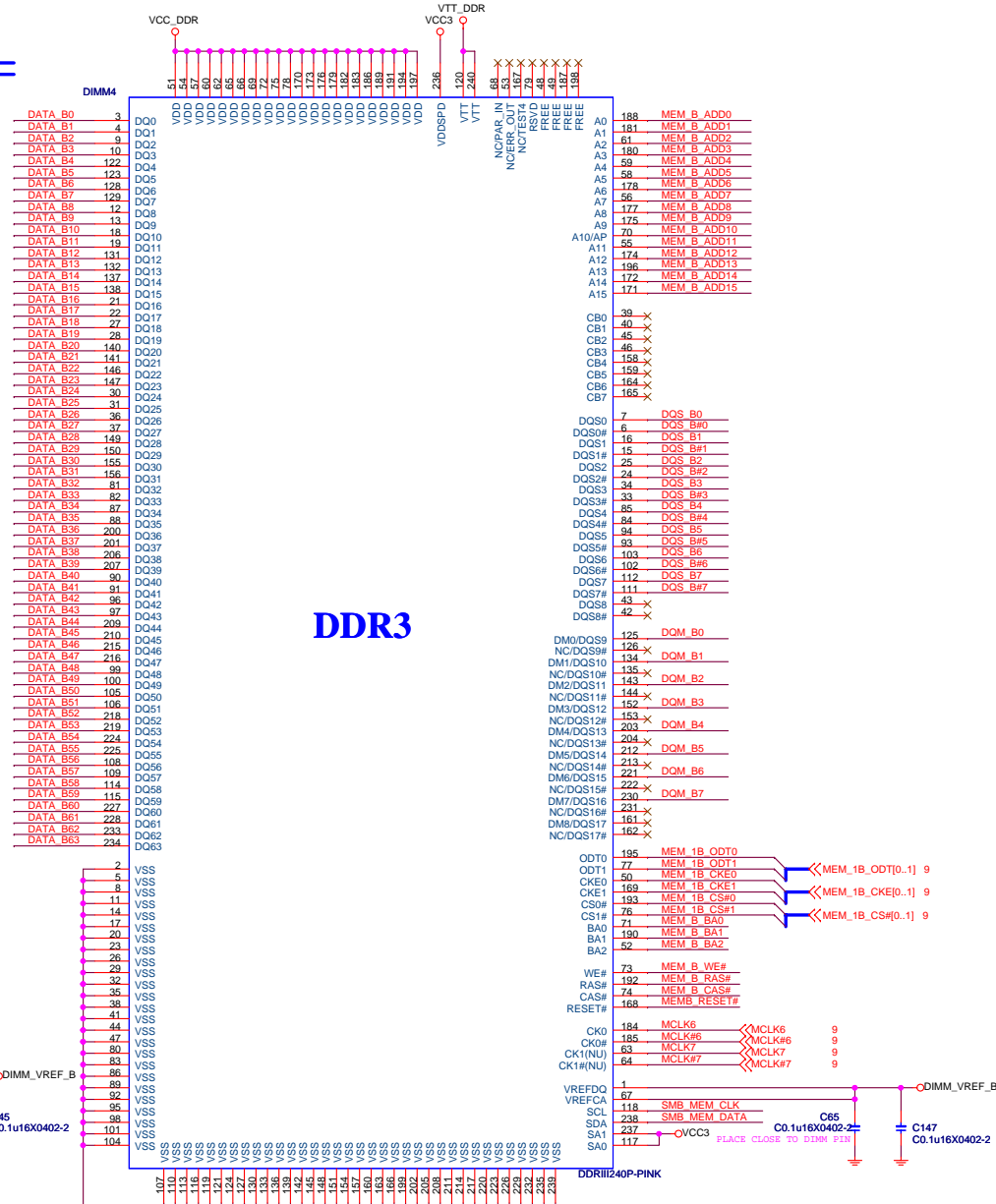
DDR3 DIMM3



Address : 001 (0xA2)

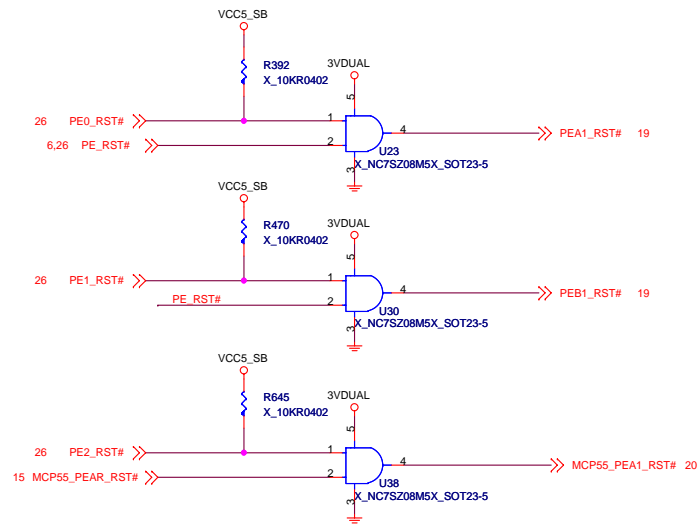


DDR3 DIMM4

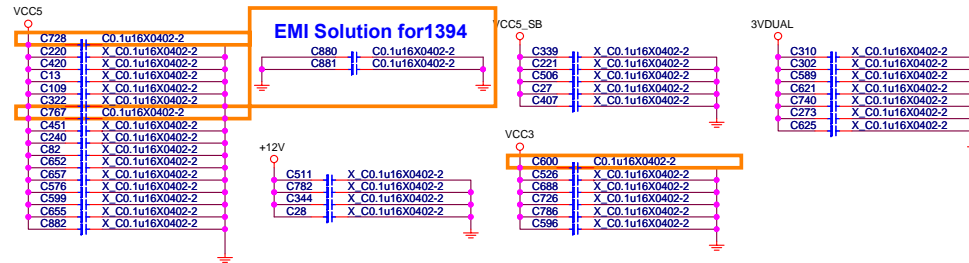


Address : 011 (0xA6)





EMI Solution 2007-10-25



MCP55 - HT / PCI / LPC

VCC1_2

C847 C0.1u16X0402-2

C848 C0.1u16X0402-2

C849 C0.1u16X0402-2

C850 C0.1u16X0402-2

C851 C0.1u16X0402-2

C852 C0.1u16X0402-2

C853 C0.1u16X0402-2

C854 C0.1u16X0402-2

C855 C0.1u16X0402-2

C856 C0.1u16X0402-2

C857 C0.1u16X0402-2

C858 C0.1u16X0402-2

C859 C0.1u16X0402-2

C860 C0.1u16X0402-2

C861 C0.1u16X0402-2

C862 C0.1u16X0402-2

Bottom Side Cap.

LPC_FRAME#

R552 8.2KR0402

LPC_FRAME#

0 : Boot ROM on LPC Bus

1 : Boot ROM on PCI Bus

LPC_CS# 8.2KR0402 R562

LPC_DRO#0 8.2KR0402 R557

SERIRQ 8.2KR0402 R545

PME# 8.2KR0402 R628

VCC3

3VDUAL

U31A

7 HTMCPU_DWN[7..0]

HTMCPU_DWN0 AK32 HT_MCP_RXD0_P

HTMCPU_DWN1 AJ32 HT_MCP_RXD1_P

HTMCPU_DWN2 AH32 HT_MCP_RXD2_P

HTMCPU_DWN3 AH30 HT_MCP_RXD3_P

HTMCPU_DWN4 AF31 HT_MCP_RXD4_P

HTMCPU_DWN5 AE32 HT_MCP_RXD5_P

HTMCPU_DWN6 AD32 HT_MCP_RXD6_P

HTMCPU_DWN7 AD30 HT_MCP_RXD7_P

AG27 HT_MCP_RXD8_P

AF27 HT_MCP_RXD9_P

AD26 HT_MCP_RXD10_P

AE29 HT_MCP_RXD11_P

AB23 HT_MCP_RXD12_P

AB26 HT_MCP_RXD13_P

AB28 HT_MCP_RXD14_P

AA28 HT_MCP_RXD15_P

Bottom Side Cap. R748 49.9R1%

7 HTMCPU_DWN[7..0]

HTMCPU_DWN0 AK31 HT_MCP_RXD0_N

HTMCPU_DWN1 AJ31 HT_MCP_RXD1_N

HTMCPU_DWN2 AH31 HT_MCP_RXD2_N

HTMCPU_DWN3 AH29 HT_MCP_RXD3_N

HTMCPU_DWN4 AF30 HT_MCP_RXD4_N

HTMCPU_DWN5 AE31 HT_MCP_RXD5_N

HTMCPU_DWN6 AD31 HT_MCP_RXD6_N

HTMCPU_DWN7 AD29 HT_MCP_RXD7_N

AG28 HT_MCP_RXD8_N

AF28 HT_MCP_RXD9_N

AD25 HT_MCP_RXD10_N

AE28 HT_MCP_RXD11_N

AB24 HT_MCP_RXD12_N

AB25 HT_MCP_RXD13_N

AB27 HT_MCP_RXD14_N

AA29 HT_MCP_RXD15_N

VCC1_2 R749 49.9R1%

Bottom Side Cap.

7 HTMCPU_DWNCLK0

7 HTMCPU_DWNCLK0#

R746 49.9R1% HT_DWNCLK1

R747 49.9R1% HT_DWNCLK1#

VCC1_2

7 HTMCPU_DWNCNTL

7 HTMCPU_DWNCNTL#

AC30 HT_MCP_RXCTL_P

AC29 HT_MCP_RXCTL_N

R420 150R1%0402 HTMCPU_COMP_GND1

R421 49.9R1%0402 HTMCPU_COMP_GND2

AG26 HT_MCP_COMP_GND1

AG25 HT_MCP_COMP_GND2

3VDUAL R419 10KR0402 MCP_THRIP#

AJ29 THERMTRIP/GPIO*

VCC1_5

VCC3

+1.5V_PLL_CPU_HT

P23

AC21 +3.3V_HT

AC22 +3.3V_PLL_CPU

AC23 +3.3V_PLL_HT

CP13 X COPPER

FB7 X 30L500mA-200-RH

+3.3V_PLL_CPU_HT

C494 C4.7u6.3X5-1

C498 C0.1u16X0402-2 C0.1u16X

C855 C0.1u16X0402-2

C480 C0.1u16X0402-2

Bottom Side Cap.

U31B

HT_MCP_TXD0_F R29 HTMCPU_UP0

HT_MCP_TXD1_F T29 HTMCPU_UP1

HT_MCP_TXD2_F T31 HTMCPU_UP2

HT_MCP_TXD3_F U31 HTMCPU_UP3

HT_MCP_TXD4_F W29 HTMCPU_UP4

HT_MCP_TXD5_F Y29 HTMCPU_UP5

HT_MCP_TXD6_F Y31 HTMCPU_UP6

HT_MCP_TXD7_F AA31 HTMCPU_UP7

R24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP_TXD0_F R30 HTMCPU_UP0

HT_MCP_TXD1_F T30 HTMCPU_UP1

HT_MCP_TXD2_F T32 HTMCPU_UP2

HT_MCP_TXD3_F U32 HTMCPU_UP3

HT_MCP_TXD4_F W30 HTMCPU_UP4

HT_MCP_TXD5_F Y30 HTMCPU_UP5

HT_MCP_TXD6_F Y32 HTMCPU_UP6

HT_MCP_TXD7_F AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP_TXD0_F R30 HTMCPU_UP0

HT_MCP_TXD1_F T30 HTMCPU_UP1

HT_MCP_TXD2_F T32 HTMCPU_UP2

HT_MCP_TXD3_F U32 HTMCPU_UP3

HT_MCP_TXD4_F W30 HTMCPU_UP4

HT_MCP_TXD5_F Y30 HTMCPU_UP5

HT_MCP_TXD6_F Y32 HTMCPU_UP6

HT_MCP_TXD7_F AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP_TXD0_F R30 HTMCPU_UP0

HT_MCP_TXD1_F T30 HTMCPU_UP1

HT_MCP_TXD2_F T32 HTMCPU_UP2

HT_MCP_TXD3_F U32 HTMCPU_UP3

HT_MCP_TXD4_F W30 HTMCPU_UP4

HT_MCP_TXD5_F Y30 HTMCPU_UP5

HT_MCP_TXD6_F Y32 HTMCPU_UP6

HT_MCP_TXD7_F AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP_TXD0_F R30 HTMCPU_UP0

HT_MCP_TXD1_F T30 HTMCPU_UP1

HT_MCP_TXD2_F T32 HTMCPU_UP2

HT_MCP_TXD3_F U32 HTMCPU_UP3

HT_MCP_TXD4_F W30 HTMCPU_UP4

HT_MCP_TXD5_F Y30 HTMCPU_UP5

HT_MCP_TXD6_F Y32 HTMCPU_UP6

HT_MCP_TXD7_F AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP_TXD0_F R30 HTMCPU_UP0

HT_MCP_TXD1_F T30 HTMCPU_UP1

HT_MCP_TXD2_F T32 HTMCPU_UP2

HT_MCP_TXD3_F U32 HTMCPU_UP3

HT_MCP_TXD4_F W30 HTMCPU_UP4

HT_MCP_TXD5_F Y30 HTMCPU_UP5

HT_MCP_TXD6_F Y32 HTMCPU_UP6

HT_MCP_TXD7_F AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP_TXD0_F R30 HTMCPU_UP0

HT_MCP_TXD1_F T30 HTMCPU_UP1

HT_MCP_TXD2_F T32 HTMCPU_UP2

HT_MCP_TXD3_F U32 HTMCPU_UP3

HT_MCP_TXD4_F W30 HTMCPU_UP4

HT_MCP_TXD5_F Y30 HTMCPU_UP5

HT_MCP_TXD6_F Y32 HTMCPU_UP6

HT_MCP_TXD7_F AA32 HTMCPU_UP7

T24 HTMCPU_UP0

T28 HTMCPU_UP1

T30 HTMCPU_UP2

U30 HTMCPU_UP3

W30 HTMCPU_UP4

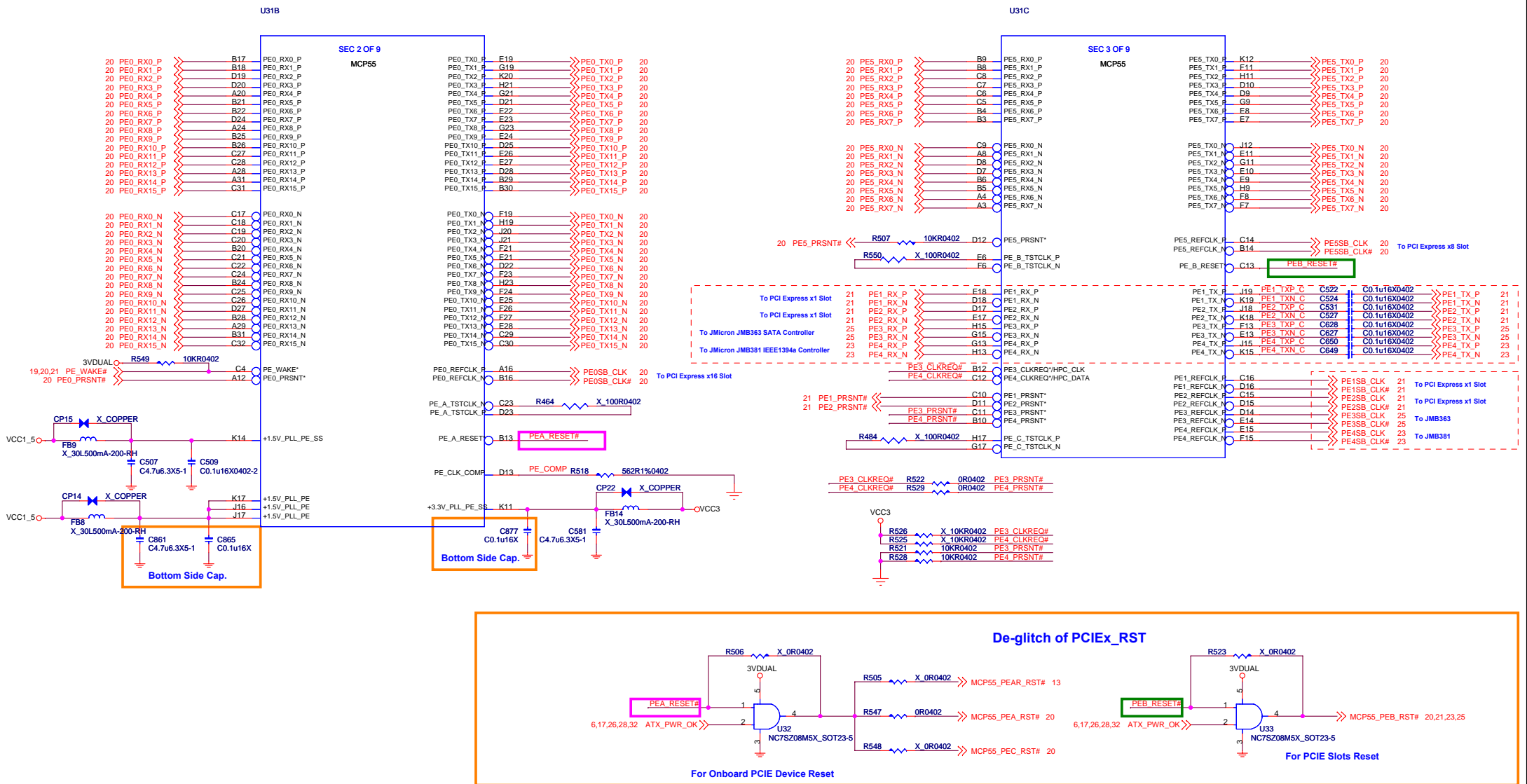
Y30 HTMCPU_UP5

Y32 HTMCPU_UP6

AA32 HTMCPU_UP7

HT_MCP

MCP55 - PCI-E



MCP55 - SATA / IDE / RGMII

Place CAP at Connector

SEC 5 OF 9

SEC 7 OF 9

SEC 8 OF 9

PATA 66/100/133 Connector

SATA1_2

SATA3_4

SATA5_6

SATA14PM_PURPLE-RH

SATA14PM_PURPLE-LH

MSI
Link to the Future

MICRO-START INT'L CO.,LTD.

Title
MCP55 - SATA / IDE / RGMII

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[illegible]

MCP55 - Audio / USB / GPIO

U31F

SEC 6 OF 9
MCP55

TP28 AG9 PROG_REFCLK
TP32 AJ8 HDA_BCLK
TP34 AH7 HDA_SDATA_OUT0/GPIO_46
TP33 AF7 HDA_SDATA_IN0/GPIO_22/MGPIO_0
TP26 AF8 HDA_SDATA_IN1/GPIO_23/MGPIO_1
TP30 AG8 HDA_SDATA_IN2/GPIO_24/MGPIO_2

HD_RESET# R575 0R0402 AG7 HDA_RESET/MGPIO_3
HD_SYNC R570 0R0402 AH8 HDA_SYNC/GPIO_44

VCC3 R465 10KR0402 AD19 GPIO_1/SLV_RDV4PWRDWN
TP24 AE19 GPIO_2/CPU_SLP/MI
TP25 AH18 GPIO_3/CPU_CLKRUN/SMI*
AE19 GPIO_4/SUS_STAT/SCI
AG17 GPIO_5/SYS_SHUTDOWN/INIT*
AD18 GPIO_6/NFERR/SYS_PERR*
AH17 GPIO_7/FERR/SYS_SERR*
AF17 GPIO_8/SMB_CLK
AJ17 GPIO_9/SMB_DATA
AF24 GPIO_10/THERM_SID1
M32 GPIO_11/CPU_VID0/RS232_SIN*
M31 GPIO_12/CPU_VID1/RS232_SOUT*
P31 GPIO_13/CPU_VID2/RS232_DTR*
N29 GPIO_14/CPU_VID3/RS232_DSR*
N28 GPIO_15/CPU_VID4/RS232_RTS*
P30 GPIO_16/CPU_VID5/RS232_CTS*
AH20 GPIO_17/SPI_DI
SB MISO AH19 GPIO_18/SPI_DO
SB MOSI AF18 GPIO_19/SPI_CS
SB SPI CS0# AF18 GPIO_20/SPI_CLK

RTC_RST# AJ22 RTC_RST*

MEM_VLD AL18 MEM_VLD
HT_VLD AE21 HT_VLD
HTVDD_EN AJ21 HTVDD_EN
VCORE_VLD AH21 CPU_VLD
VCORE_EN AG21 CPUVDD_EN

Bottom Side Cap.

VCC1_5

C623 C47u6.3X5-1
C622 C0.1u16X0402-2

MEM_VLD R504 0R0402 SLP_S5#
X_C0.1u16X0402-2 C568
HTVDD_EN R503 0R0402 HT_VLD
X_C0.1u16X0402-2 C560
VCORE_EN R487 0R0402 VCORE_VLD
X_C0.1u16X0402-2 C521

VCC5_SB R5 4.7KR0402
R42 X_1KR1%0402
Q2 X_N-MMBT3904_NL_SOT23
Q6 X_N-MMBT3904_NL_SOT23
C29 X_C0.1u16X0402-2

USB0_F AL1 USBP0 31
USB0_N AL2 USBN0 31
USB1_F AK1 USBP1 31
USB1_N AK2 USBN1 31
USB2_F AJ1 USBP2 31
USB2_N AJ2 USBN2 31
USB3_F AJ5 USBP3 31
USB3_N AJ4 USBN3 31
USB4_F AH1 USBP4 31
USB4_N AH2 USBN4 31
USB5_F AH4 USBP5 31
USB5_N AH3 USBN5 31
USB6_F AG4 USBP6 31
USB6_N AG3 USBN6 31
USB7_F AG5 USBP7 31
USB7_N AG6 USBN7 31
USB8_F AF3 USBP8 31
USB8_N AF2 USBN8 31
USB9_F AF4 USBP9 31
USB9_N AF5 USBN9 31

USB_OC0/GPIO AE4 USB_OCP#0 31
USB_OC1/GPIOMGPIO AF6 USB_OCP#2 31
USB_OC2/GPIOMGPIO AE3 USB_OCP#4 31
USB_OC3/GPIOMGPIO AE1 USB_OCP#6 31
USB_OC4/GPIOMGPIO AE2 USB_OCP#8 31
USB_RBIAS_GND AK3 USB_RBIAS_GND R579 825R1%
A20GATE/GPIO AB9 INTRUDER# A20GATE 26
INTRUDER# AL21 LPC_SMI# R621 4.7KR0402
EXT_SMI/GPIO AC4 RIF/GPIO AF9
SPKR AD9
PWRBTN# AF10
SIO_PME/GPIO AC3 SIO_PME# 26
KBRDRSTN/GPIO AB8 KBRST# 26

SMB_CLK AL20 SMB_MEM_CLK 11,12
SMB_DATA AK20 SMB_MEM_DATA 11,12
SMB_CLK AK19 SMB_CLK 19,20,21,25,28,29,30
SMB_DATA AJ19 SMB_DATA 19,20,21,25,28,29,30
+3.3V_VBAT AD21 SIOCLK 24M
BUF_SIO_CLK AD3 SUS_CLK
SUS_CLK/GPIO AD2 SUS_CLK
THERM/GPIO AD8
RSTBTN# AD10 THERM# FP_RST# 26
SLP_S5 AK18 SLP_S5# 28,31
SLP_S3 AJ18 SLP_S3# 26,28,31
PWRGD_SE AK21 RSMRST# 22,26

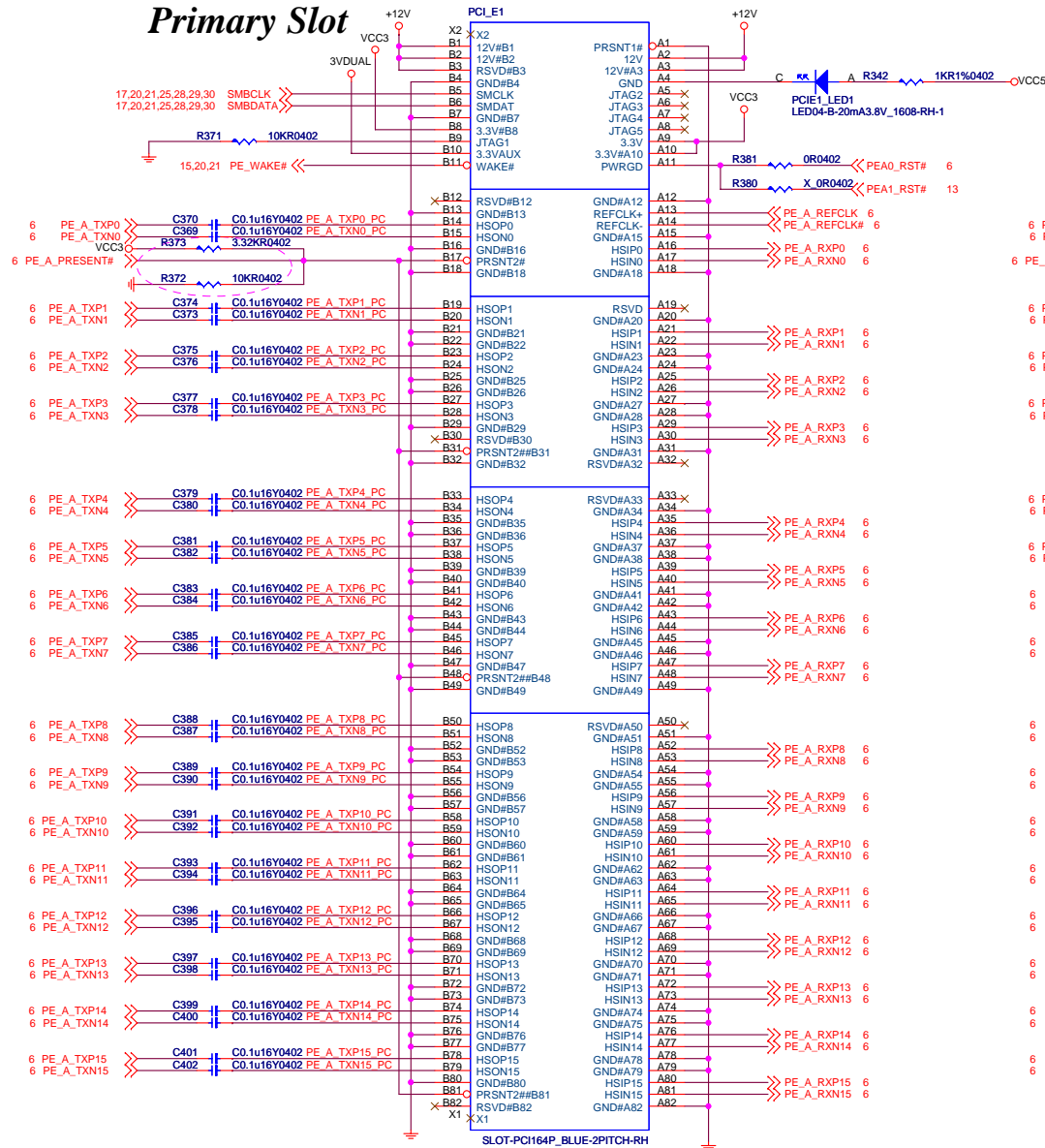
FANRPM/GPIO AD6 TP29
FANCTL/GPIO AD5 TP31
FANCTL/GPIO AD7 TP27
THERM_SIG/GPIO AK30
THERM_SID/GPIO AH27 TP23

TEST_MODE_EN P24 SB_TEST R438 1KR1%

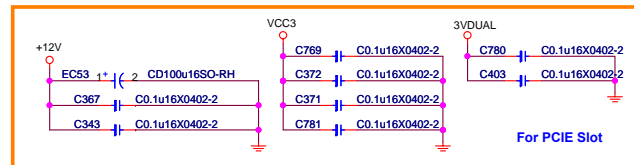
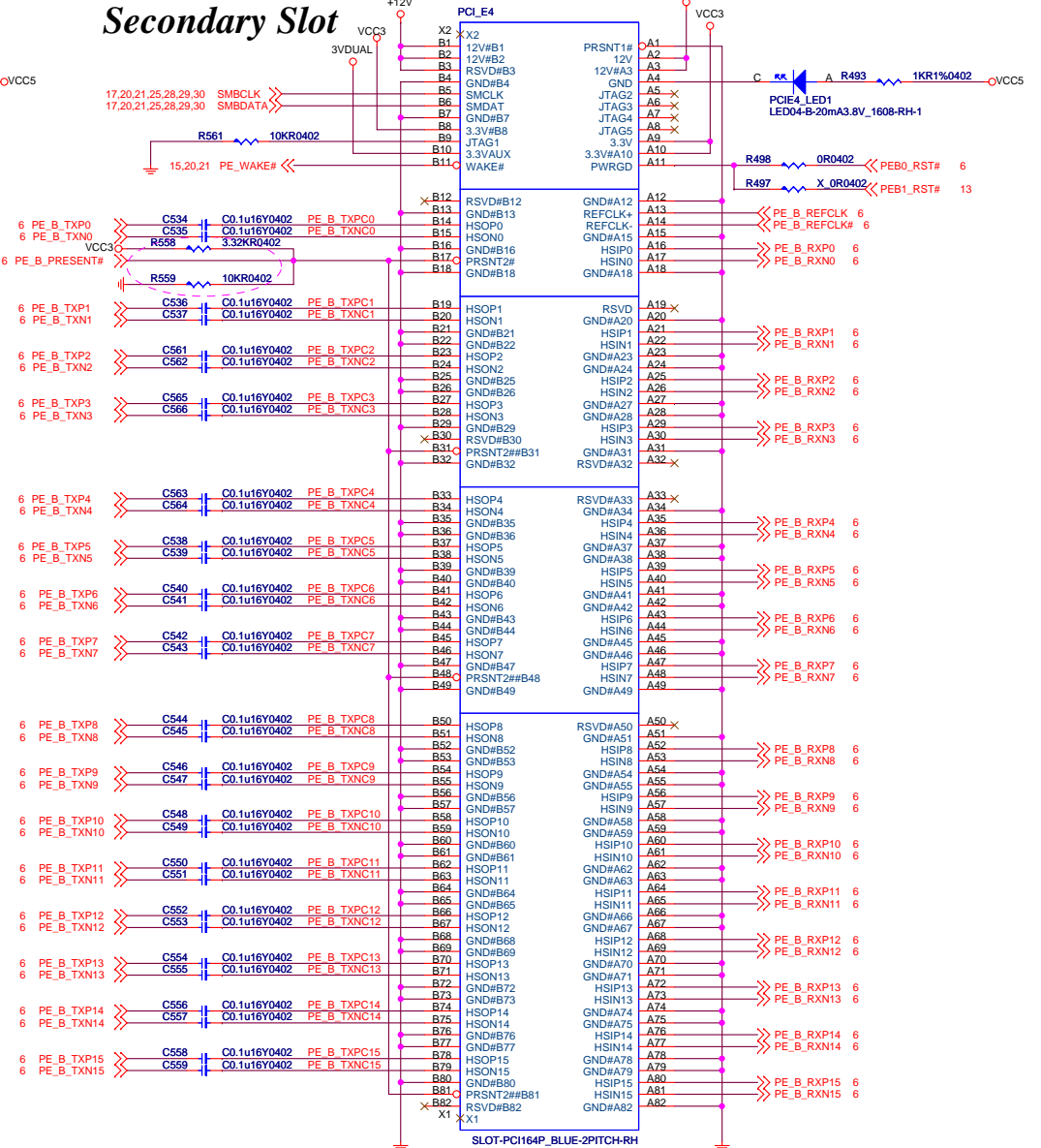
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PCI-Express x16 Primary and Secondary Slot

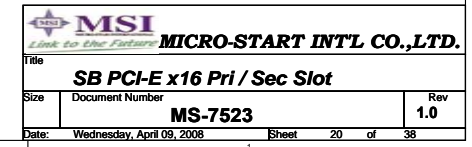
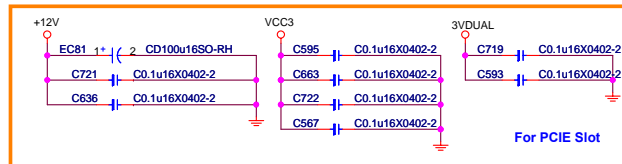
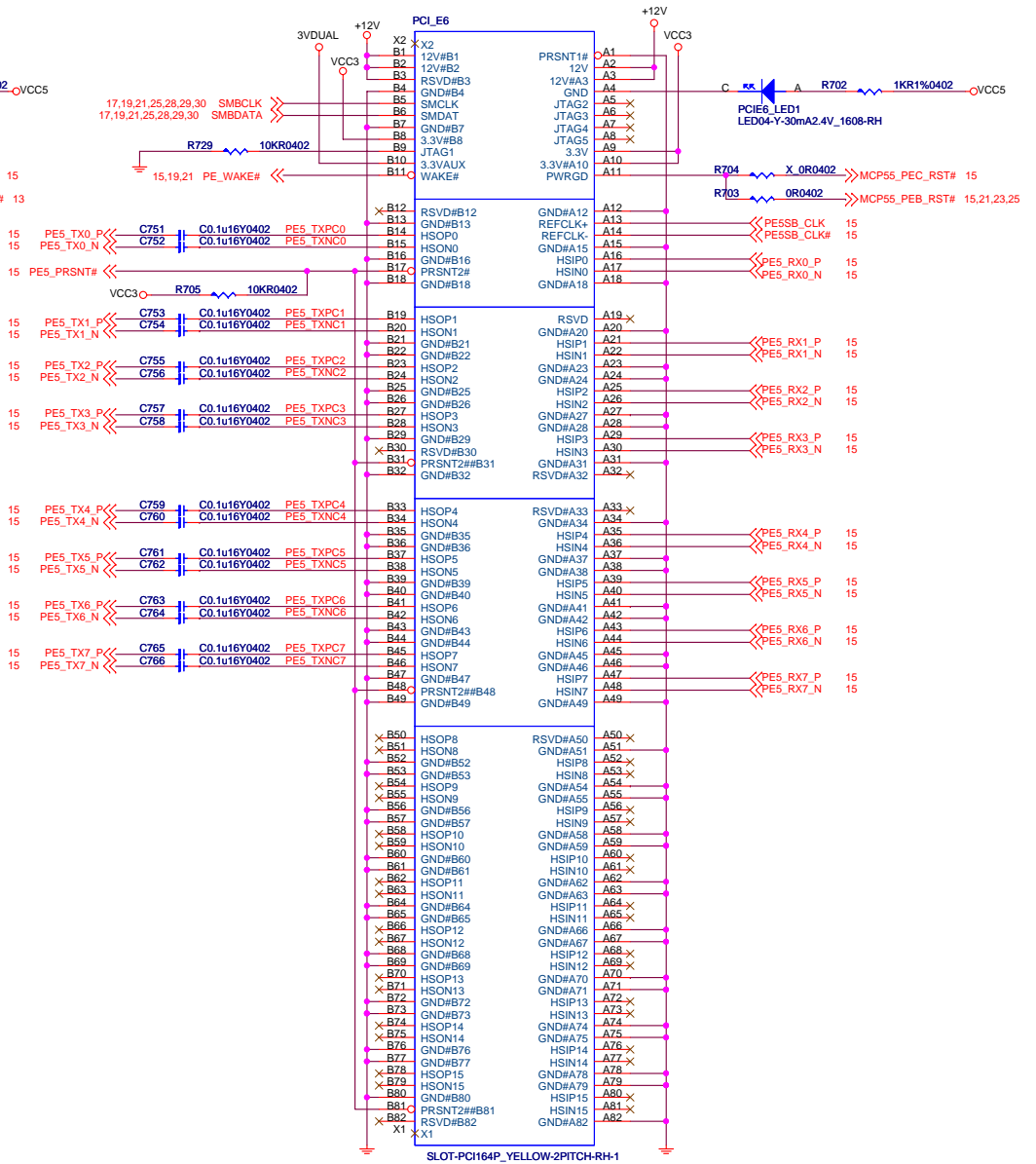
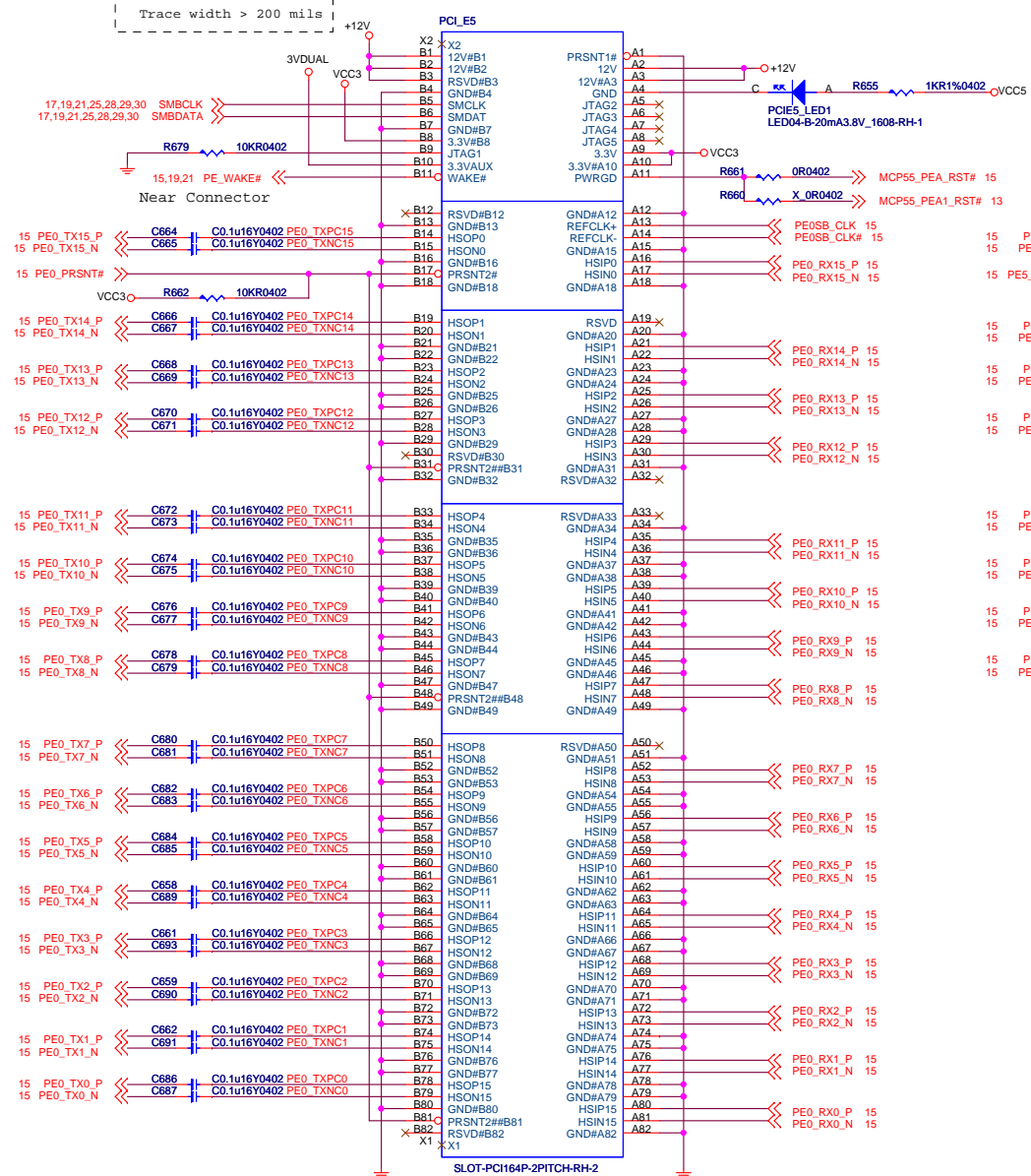
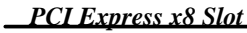
Primary Slot



Secondary Slot

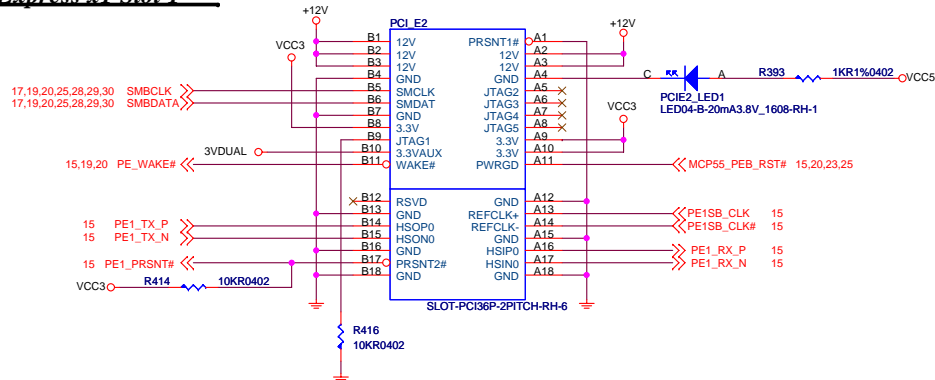


SB PCI Express x16 Slot and PCI Express x8 Slot

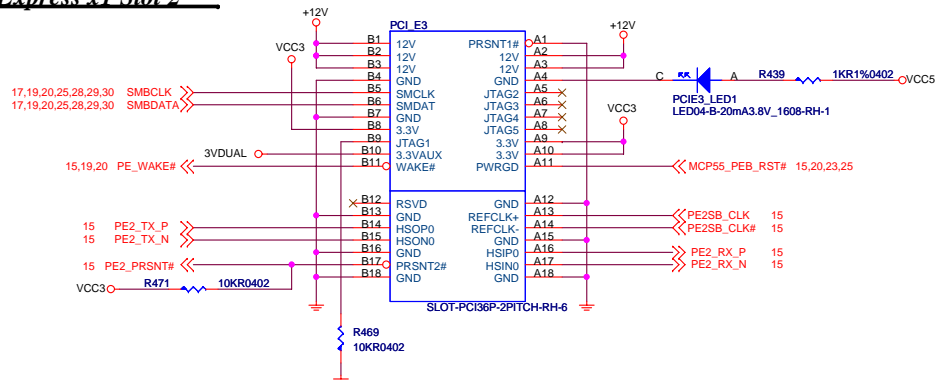


SB PCI-Express x1 Slots and PCI Slot

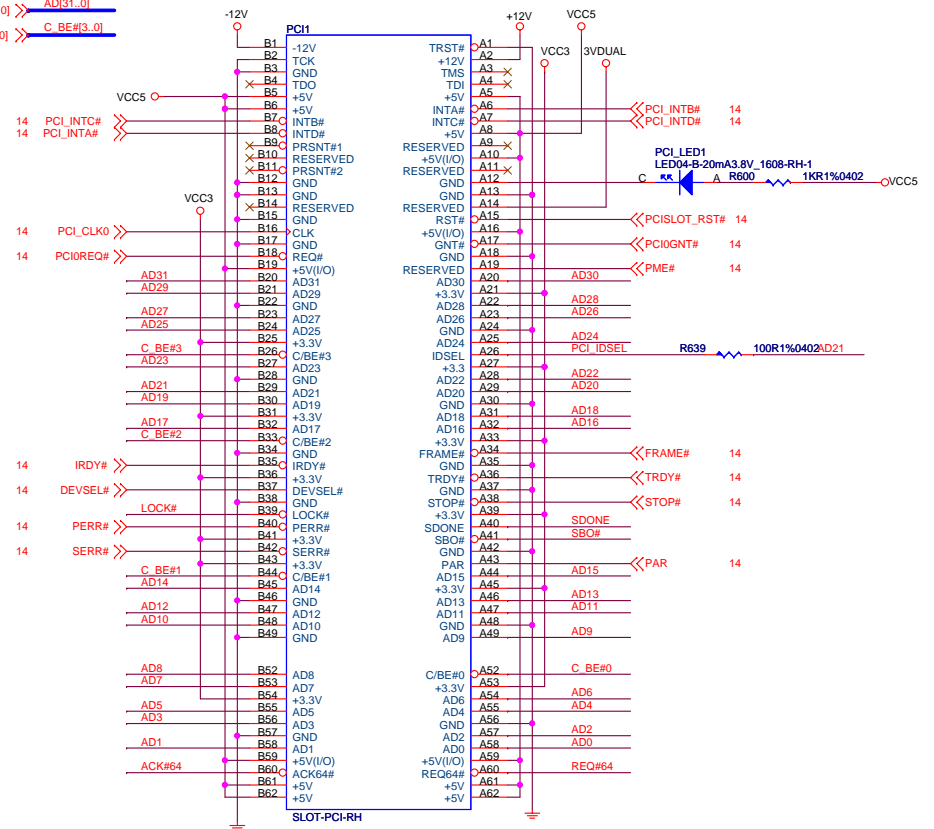
PCI Express x1 Slot 1



PCI Express x1 Slot 2

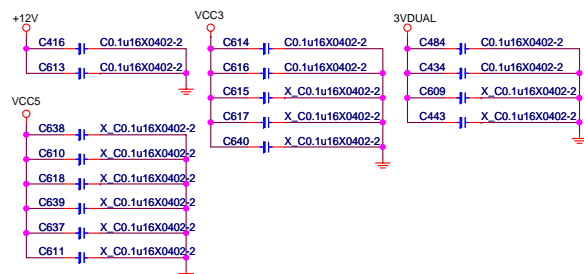


PCI Slot 1 (PCI VER: 2.2 Comply)

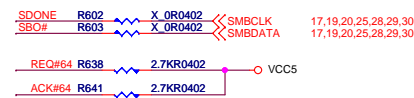
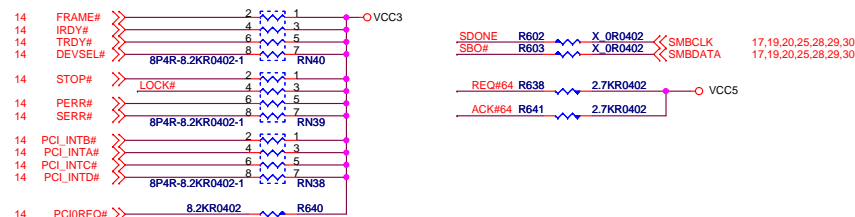


```
IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*
```

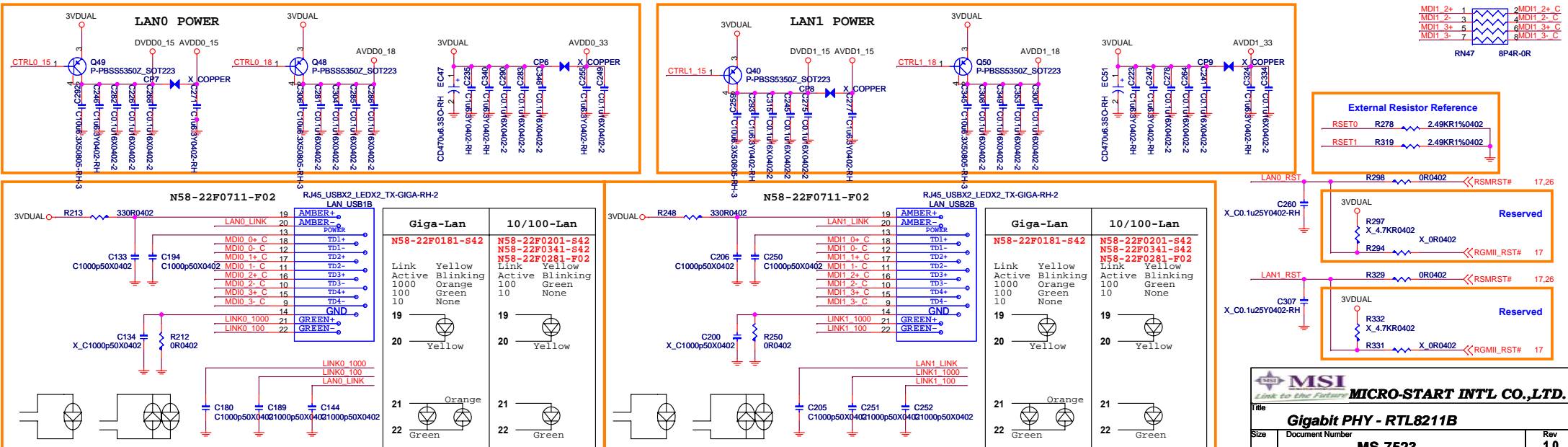
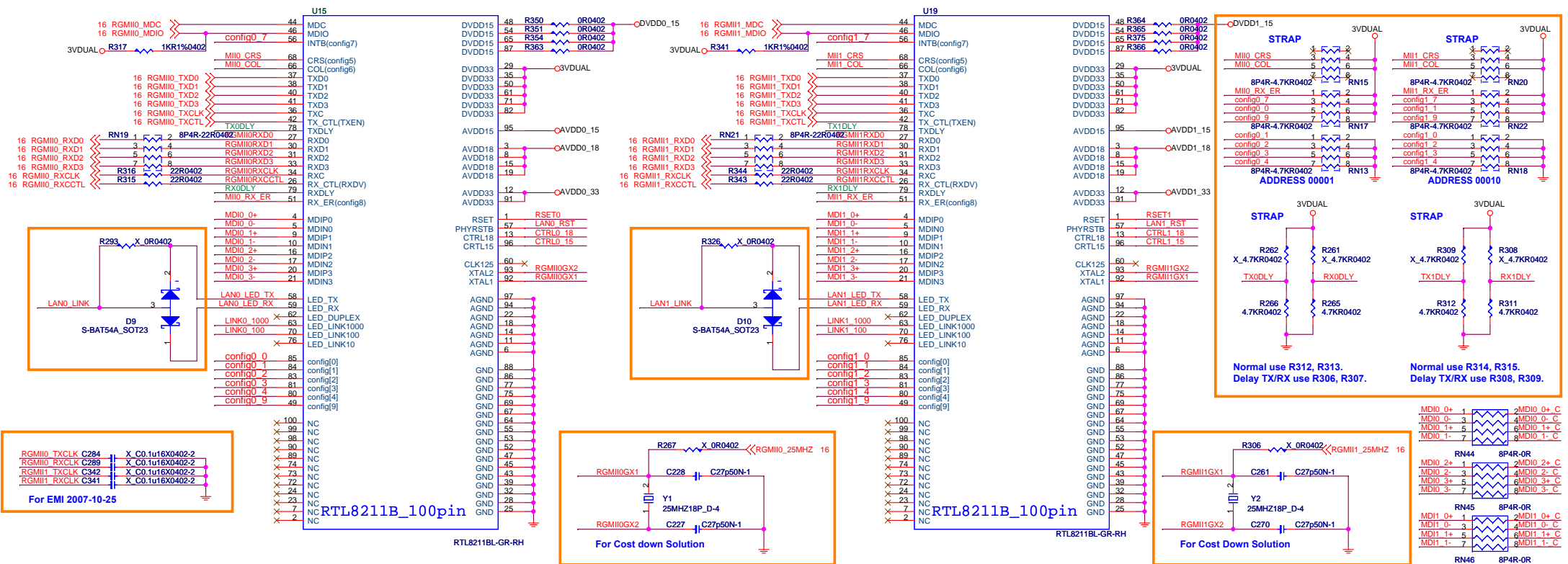
PCI Slot Decoupling Capacitors



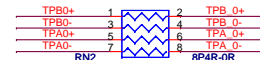
PCI Pull Up / Down Resistors




RTL8211B RGMII Gigabit PHY (Lan 1 and Lan 2)



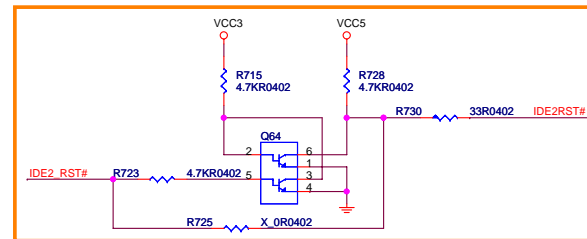
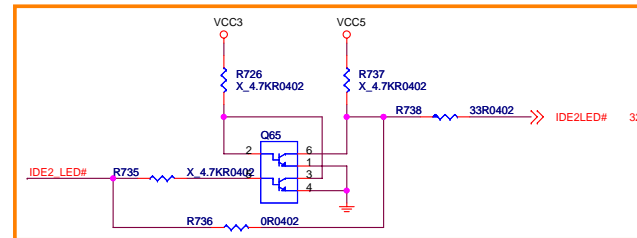
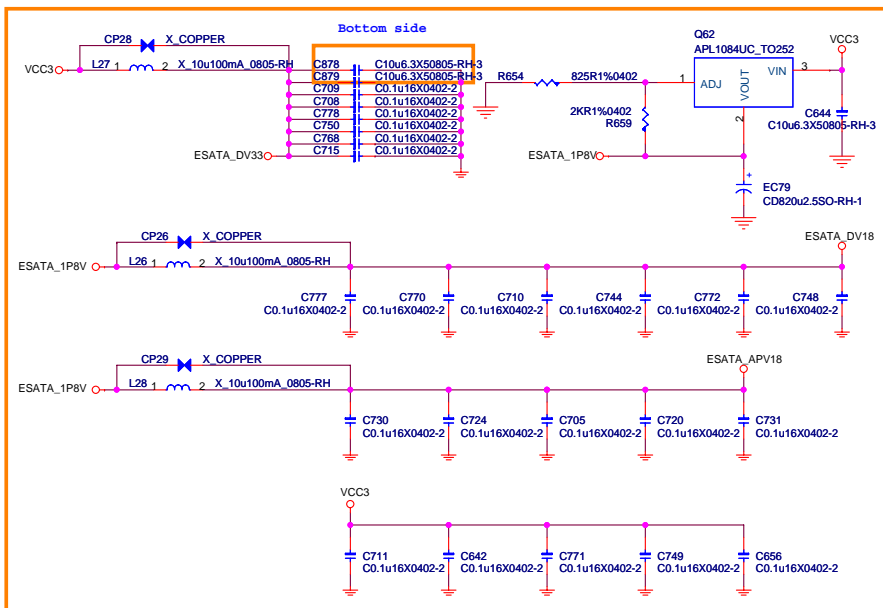
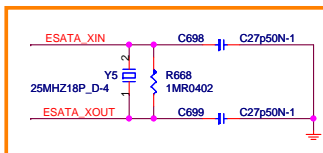
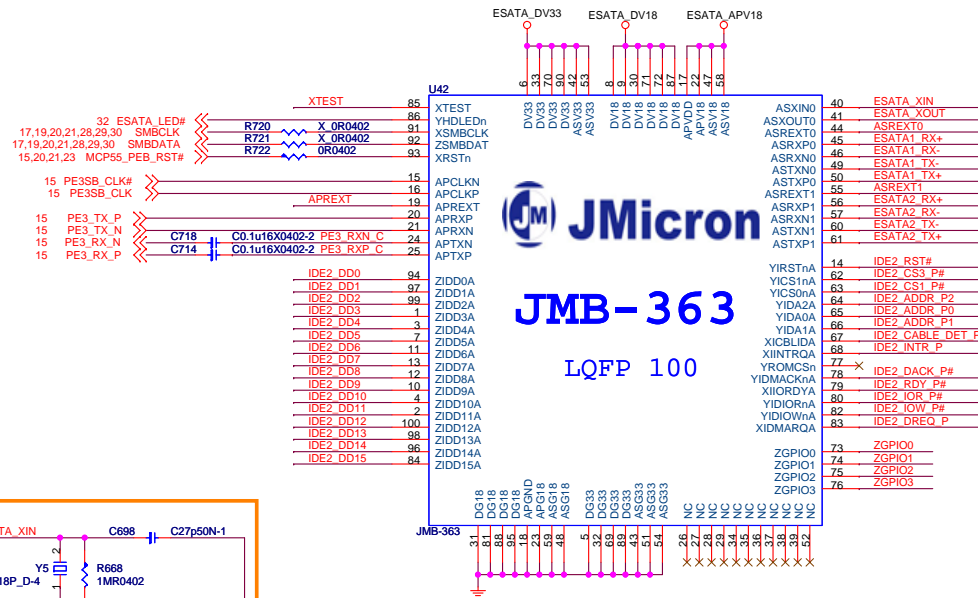
JMB381



Azalia Codec - ALC888

| | | |
|---|-----------------------------------|-------------------|
|  MICRO-START INT'L CO.,LTD. | | |
| Title Azalia Codec - ALC888 | | |
| Size | Document Number MS-7523 | Rev 1.0 |
| Date: Wednesday, April 09, 2008 | | |
| Sheet 24 of 38 | | |

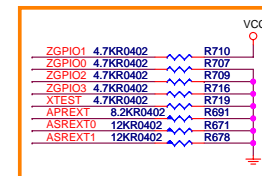
JMicron JMB363 eSATA Controller



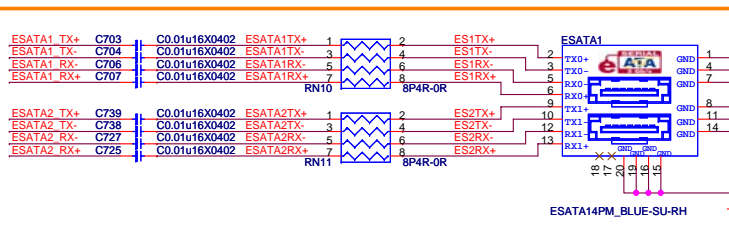
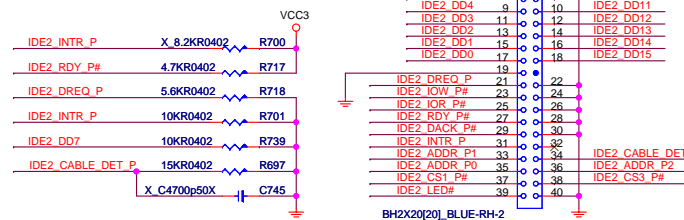
SATA II Port 0 External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground ASG18 (pin#48).

SATA II Port 0 External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground ASG18 (pin#59).

PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18).



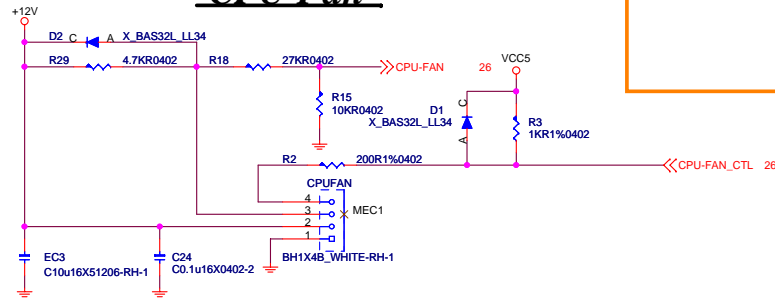
PATA 66/100/133 Connector



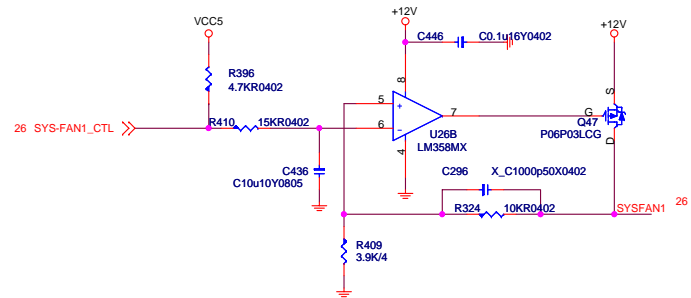
JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function
JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0
JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.
JMB363 GPIO3
Reserved for debugging.
JMB363 Test Mode Enable.
High-active signal to enable testing and debug modes of JMB363.

Fan Controller

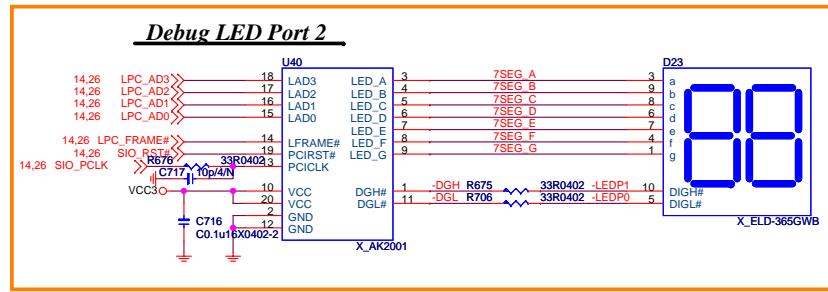
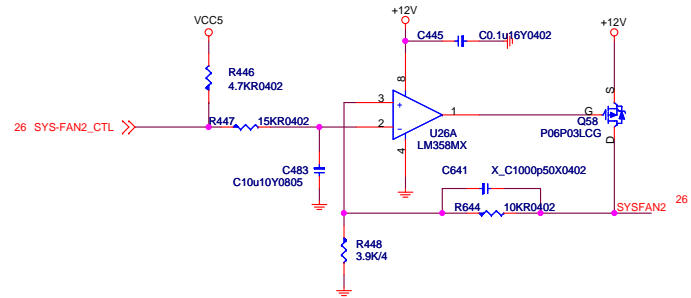
CPU Fan



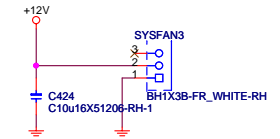
System Fan 1



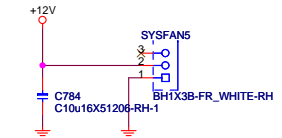
System Fan 2



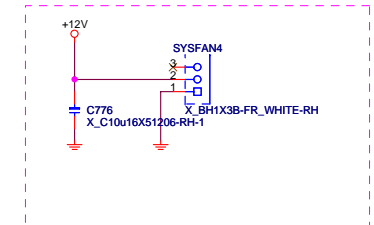
System Fan 3



System Fan 4

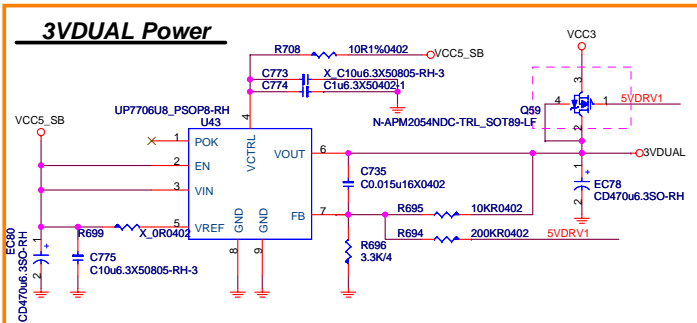


System Fan 5



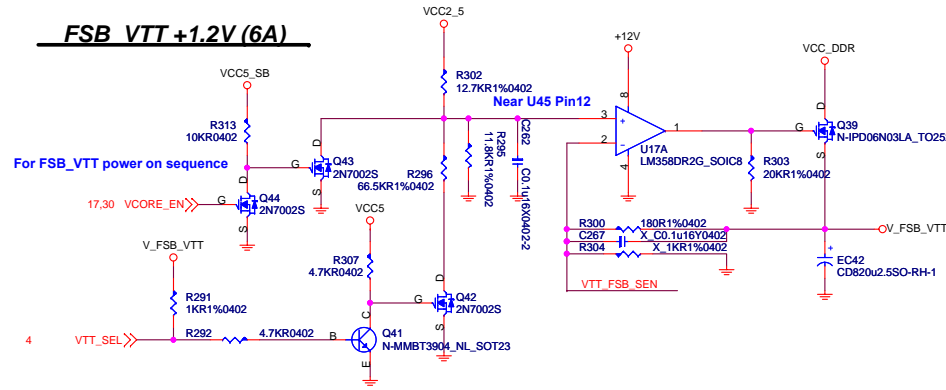
uPL ACPI Solution

3VDUAL Power

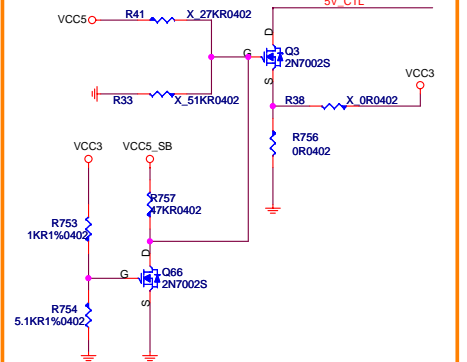


FSB VTT +1.2V (6A)

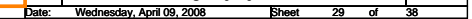
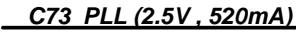
For FSB_VTT power on sequence



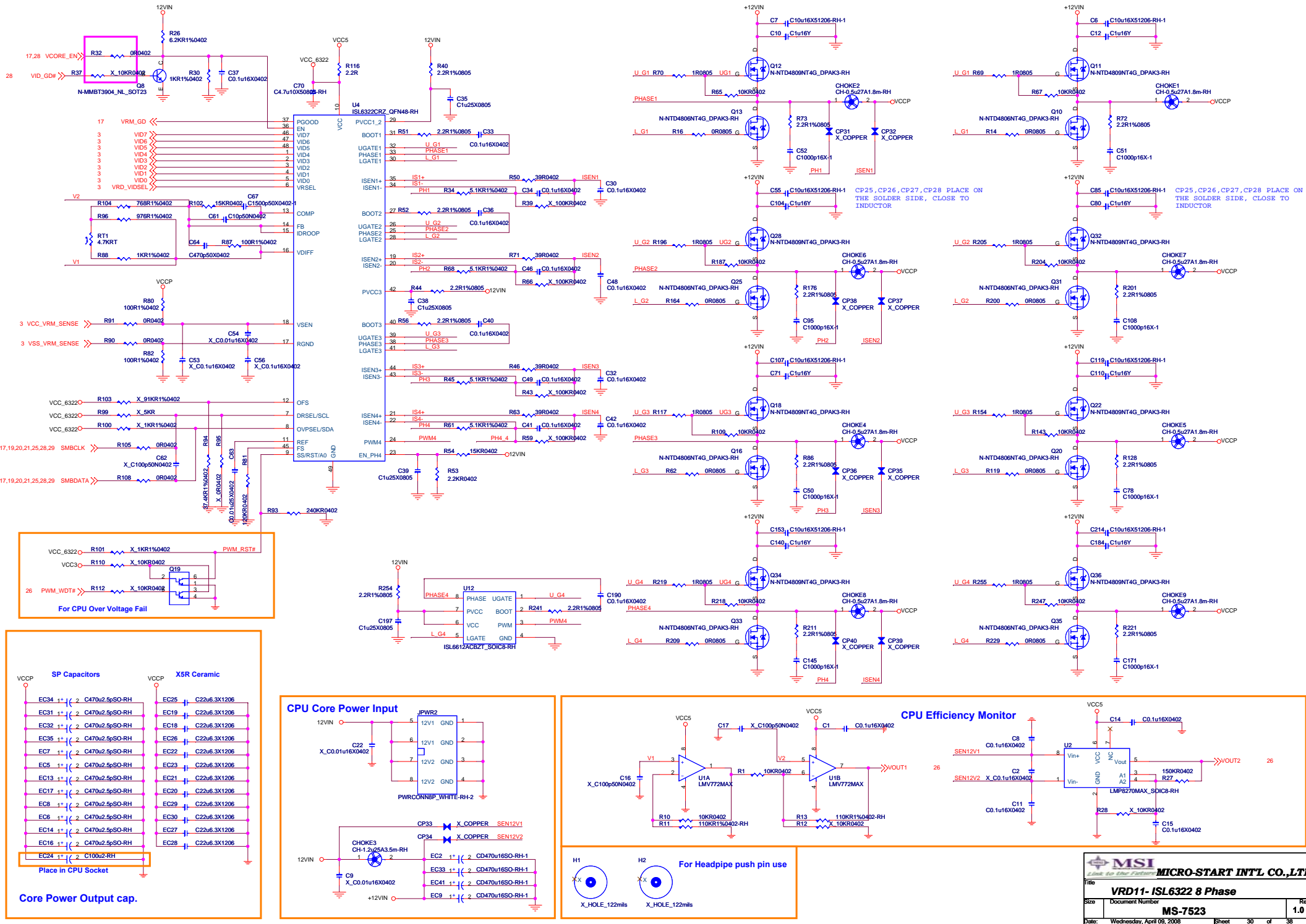
UPI Suggest



C73 1.3V Core Power (25 A)

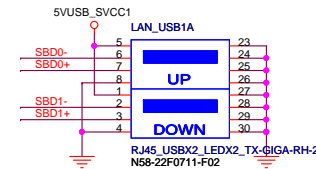
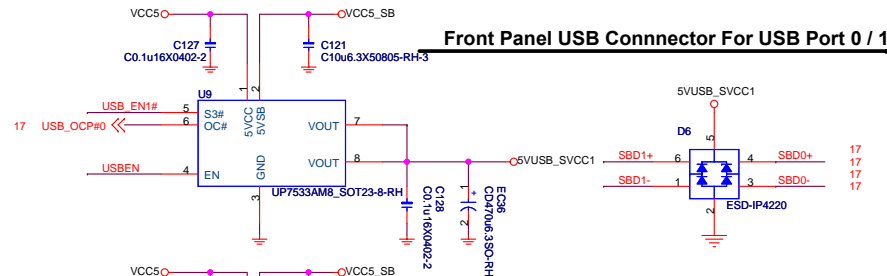


Voltage Regular Module (VRD11)

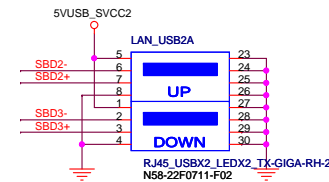
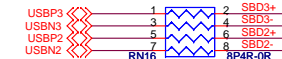
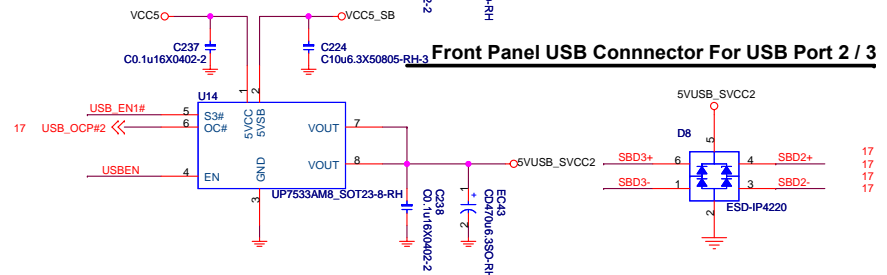


Front Panel and Real I/O USB Connector

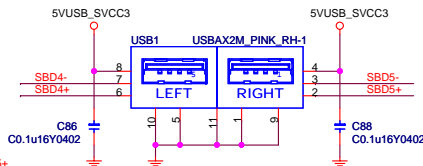
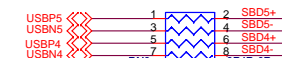
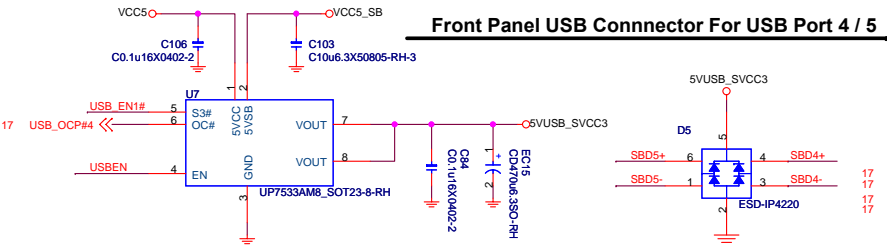
Front Panel USB Connector For USB Port 0 / 1



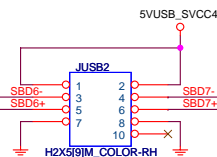
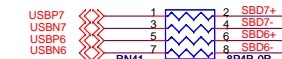
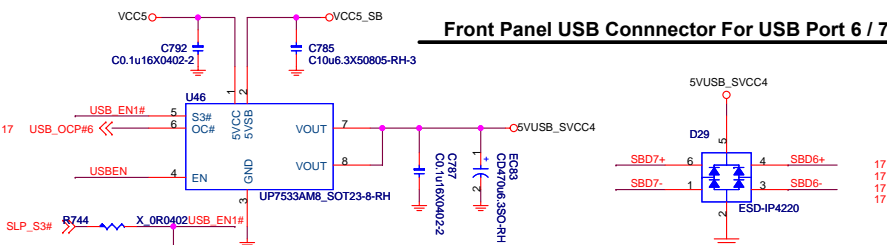
Front Panel USB Connector For USB Port 2 / 3



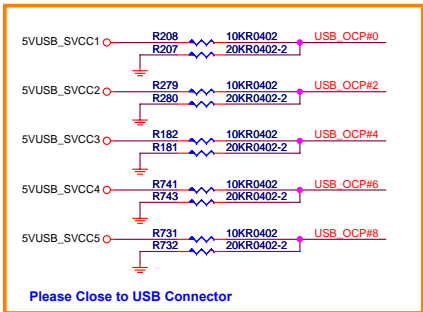
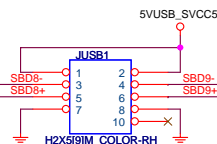
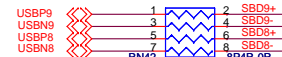
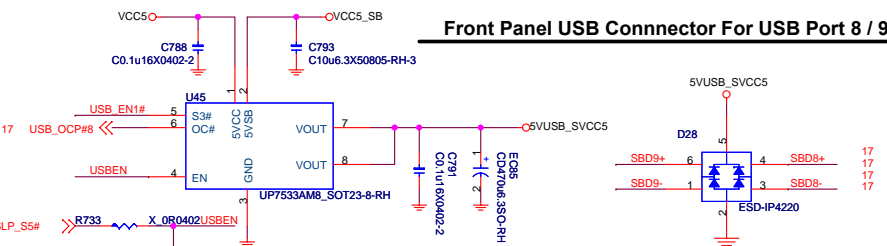
Front Panel USB Connector For USB Port 4 / 5

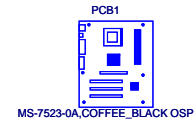
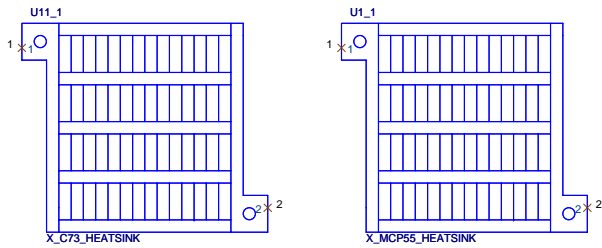


Front Panel USB Connector For USB Port 6 / 7

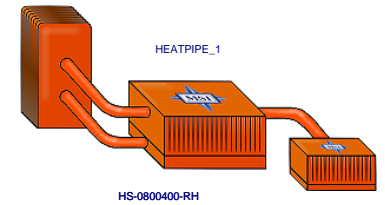


Front Panel USB Connector For USB Port 8 / 9



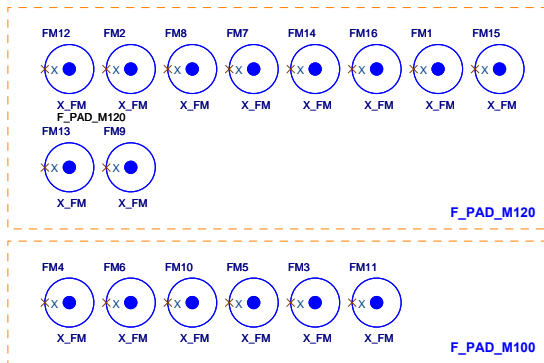


PD0-075100A-D05
PD0-075100A-Y34

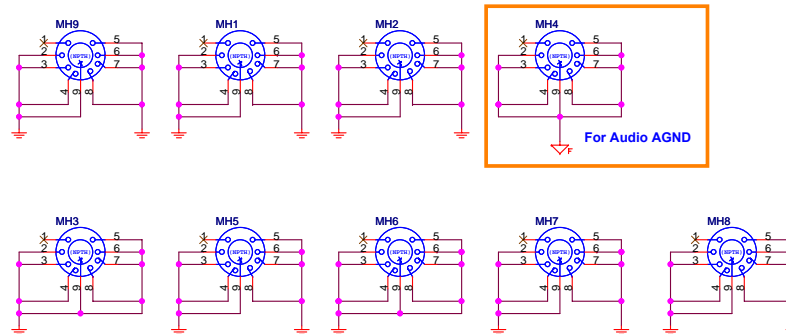


Simulation

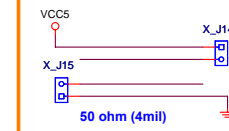
Optics Orientation Holes



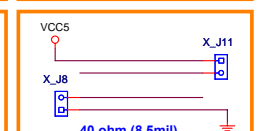
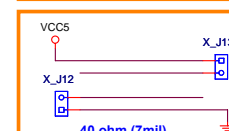
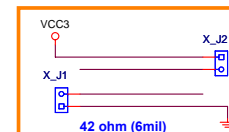
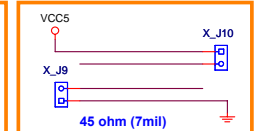
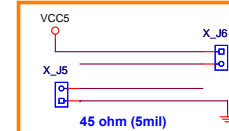
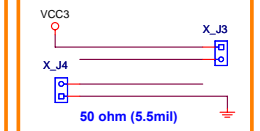
PCB Mounting Holes



Top and Bottom layer

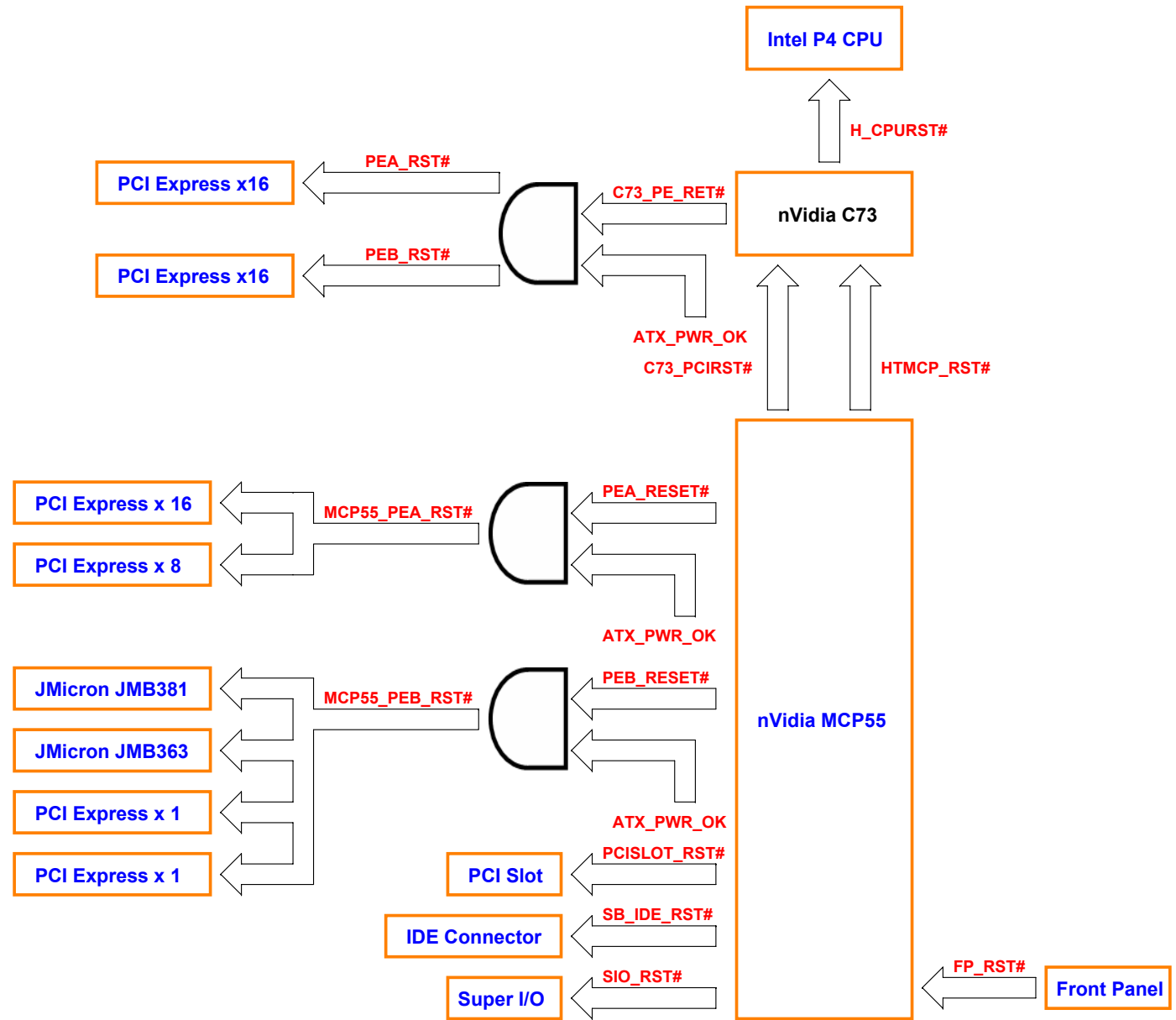


INT1 and INT2 layer

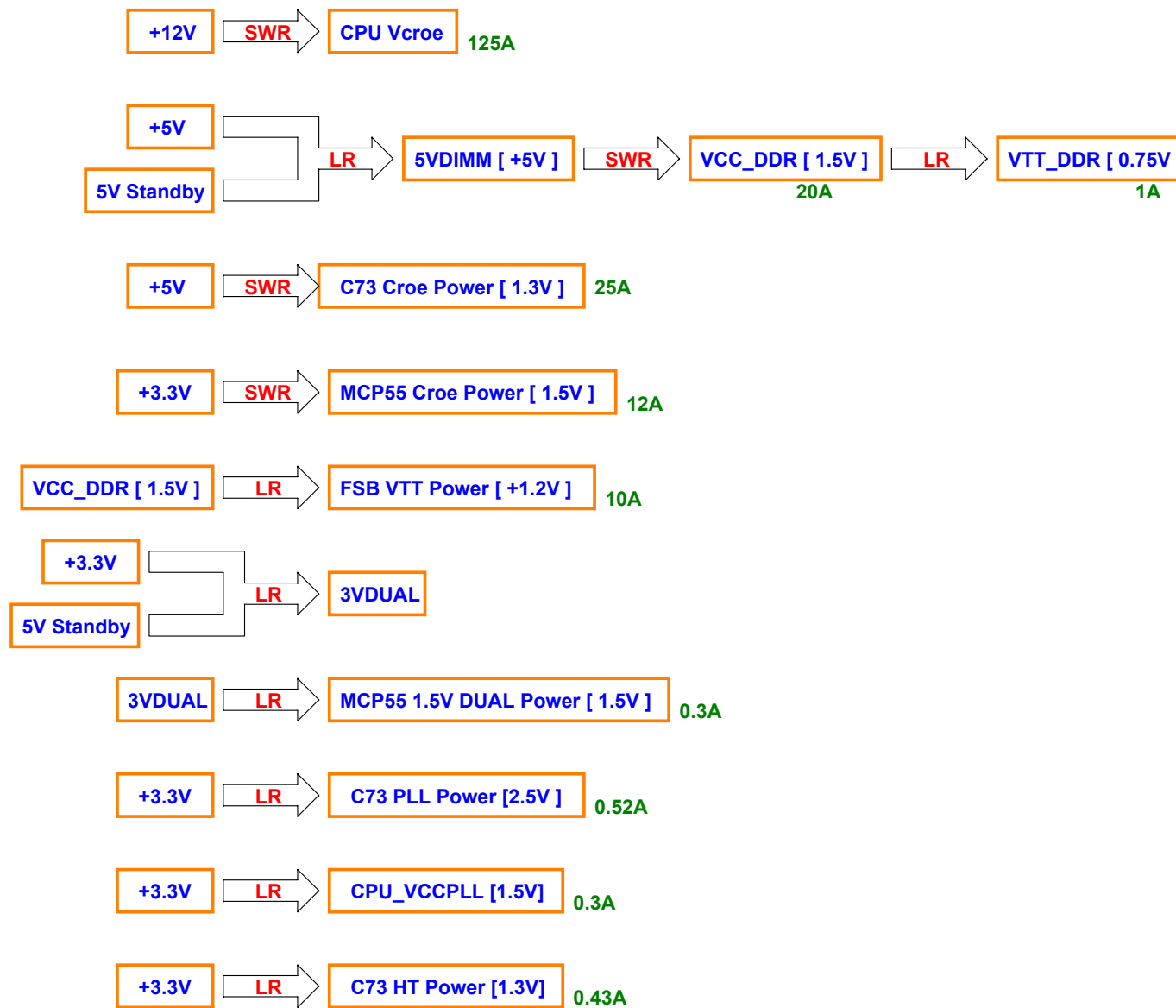


Power On/Off Sequence

System Reset Map



Syatem Power Map



Configuration & GPIO

PCI Configuration

| DEVICE | MCP1 INT Pin | REQ#/GNT# | IDSEL | CLOCK | PCI Reset |
|------------|--------------|----------------------|-------|----------|--------------|
| PCI slot 1 | PIRQ#A | PCIOREQ# PCIOGNT# | AD21 | PCI_CLK0 | PCISLOT_RST# |

DDRII DIMM Configuration

| DIMM1 | DIMM2 | DIMM3 | DIMM4 |
|-------------|-------------|-------------|-------------|
| A0 1010000B | A4 1010010B | A2 1010001B | A6 1010011B |
| 0A | 0B | 1A | 1B |

SMBus Distribution

| SMBus | Power | Load |
|-----------------------------|---------|--|
| SMBDATA SMBCLK | VCC3 | MCP55 , JM363 , PWM , Super I/O , uPI Power IC PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot |
| SMB_MEM_DATA SMB_MEM_CLK | VCC3_SB | MCP55 |

System Reset Signal

| Signal | Device |
|--------------|--|
| PE_RESET# | |
| H_CPURST# | CPU |
| HTMCP_RST# | C73 |
| PE_A_RESET# | C73 PCI Express x 16 Primary Slot |
| PE_B_RESET# | C73 PCI Express x 16 Secondary Slot |
| PEB_RESET# | JMicron JMB363 eSATA Controller JMicron JMB381 IEEE 1394a Host Controller MCP55 PCI Express x 1 Slot |
| PEA_RESET# | MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot |
| PCISLOT_RST# | MCP55 PCI Slot |
| C73_PCIRST# | C73 |
| SB_IDE_RST# | Master IDE Connector |
| SIO_RST# | Super I/O |

SuperI/O GPIO Function

| Pin Name | Function Description |
|----------|--------------------------|
| GP4 | CPU_GTL_REF Select |
| GP5 | Reset PWM |
| SLOT0CC# | Detect CPU remove or not |
| COPEN# | Detect Case Open or not |

MCP55 GPIO Function

| Pin Name | Function Description |
|----------|--------------------------|
| GP10 | USB Connector OC# Detect |

Device Clock Signal

| Signal | Device |
|--|--|
| CK_H_CPU# CK_H_CPU | C73 to CPU |
| HTMCP_DWNCLK0 HTMCP_DWNCLK0# | C73 to MCP55 |
| HTMCP_UPCLK0 HTMCP_UPCLK0# | MCP55 to C73 |
| PE_A_REFCLK PE_A_REFCLK# | C73 to Express x 16 Primary Slo |
| PE_B_REFCLK PE_B_REFCLK# | C73 to Express x 16 Secondary Slot |
| | |
| MCPOUT_200MHZ MCPOUT_200MHZ# | MCP55 to C73 |
| C73_25MHZ | MCP55 to C73 |
| PE0SB_CLK PE0SB_CLK# | MCP55 to Express x 16 Slot |
| PE5SB_CLK PE5SB_CLK# | MCP55 to Express x 8 Slot |
| PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK# | MCP55 to PCI Express x 1 Slot |
| PE3SB_CLK PE3SB_CLK# | MCP55 to JMicron JMB363 eSATA Controller |
| PE4SB_CLK PE4SB_CLK# | MCP55 to JMicron JMB381 IEEE1394a Controller |
| PCI_CLK0 | MCP55 to PCI Slot |
| SIO_PCLK | MCP55 to FinTek 71883FG Super I/O |
| LPC_PCLK | MCP55 to JTPM Pin Header |

2007-11-05
Create First Version Schematic

2007-11-10
7523 0A Net-in

2007-11-07
Update project Spec.
From PDC42819 change to JMB363


2007-11-22
Update nVidia PCI Express clock jitter issue solution

2007-11-23
Gerber Out 0A

2007-11-25
Assembly

2007-12-15
HW gat sample board

2008-02-15
Gerber Out 1.0



MICRO-START INT'L CO.,LTD.

Title

History

Size

Document Number

Rev

MS-7523

1.0

Date:

Wednesday, April 09, 2008

Sheet

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of

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